

# BOXER-8310AI

---

Compact Fanless Embedded AI@Edge Box PC

User's Manual 1<sup>st</sup> Ed

## Copyright Notice

---

This document is copyrighted, 2019. All rights are reserved. The original manufacturer reserves the right to make improvements to the products described in this manual at any time without notice.

No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means without the prior written permission of the original manufacturer. Information provided in this manual is intended to be accurate and reliable. However, the original manufacturer assumes no responsibility for its use, or for any infringements upon the rights of third parties that may result from its use.

The material in this document is for product information only and is subject to change without notice. While reasonable efforts have been made in the preparation of this document to assure its accuracy, AAEMON assumes no liabilities resulting from errors or omissions in this document, or from the use of the information contained herein.

AAEMON reserves the right to make changes in the product design without notice to its users.

## Acknowledgement

---

All other products' name or trademarks are properties of their respective owners.

- Microsoft Windows is a registered trademark of Microsoft Corp.
- Intel, Pentium, and Celeron are registered trademarks of Intel Corporation
- Movidius, Myriad and Myriad X are registered trademarks of Intel Corporation
- ITE is a trademark of Integrated Technology Express, Inc.
- IBM and VGA are trademarks of International Business Machines Corporation.

All other product names or trademarks are properties of their respective owners. No ownership is implied or assumed for products, names or trademarks not herein listed by the publisher of this document.

## Packing List

---

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
BOXER-8310AI with built-in Intel Myriad X	1
3 Pin DC-In Power Connector	1
Wallmount bracket	2

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

---

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page on [AAEON.com](http://AAEON.com) for the latest version of this document.

## Safety Precautions

---

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
  - i. Damaged power cord or plug
  - ii. Liquid intrusion to the device
  - iii. Exposure to moisture
  - iv. Device is not working as expected or in a manner as described in this manual
  - v. The device is dropped or damaged
  - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

## FCC Statement

---

### **Warning!**



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

### **Caution:**

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

### **Attention:**

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*



## China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量 AAEON System

QO4-381 Rev.A0

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	×	○	○	○	○	○
外部信号 连接器及线材	×	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	×	○	○	○	○	○
硬盘	×	○	○	○	○	○
液晶模块	×	×	○	○	○	○
光驱	×	○	○	○	○	○
触控模块	×	○	○	○	○	○
电源	×	○	○	○	○	○
电池	×	○	○	○	○	○

本表格依据 SJ/T 11364 的规定编制。

○：表示该有毒有害物质在该部件所有均质材料中的含量均在  
GB/T 26572标准规定的限量要求以下。

×：表示该有害物质的某一均质材料超出了GB/T 26572的限量要求，然而该部件  
仍符合欧盟指令2011/65/EU 的规范。

备注：

- 一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
- 二、上述部件物质中央处理器、内存、硬盘、光驱、电源为选购品。
- 三、上述部件物质液晶模块、触控模块仅一体机产品适用。

# China RoHS Requirement (EN)

## Hazardous and Toxic Materials List

AAEON System

QQ4-381 Rev.A0

Component Name	Hazardous or Toxic Materials or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated biphenyls (PBBS)	Polybrominated diphenyl ethers (PBDEs)
PCB and Components	X	O	O	O	O	O
Wires & Connectors for Ext. Connections	X	O	O	O	O	O
Chassis	O	O	O	O	O	O
CPU & RAM	X	O	O	O	O	O
HDD Drive	X	O	O	O	O	O
LCD Module	X	X	O	O	O	O
Optical Drive	X	O	O	O	O	O
Touch Control Module	X	O	O	O	O	O
PSU	X	O	O	O	O	O
Battery	X	O	O	O	O	O

This form is prepared in compliance with the provisions of SJ/T 11364.

O: The level of toxic or hazardous materials present in this component and its parts is below the limit specified by GB/T 26572.

X: The level of toxic of hazardous materials present in the component exceed the limits specified by GB/T 26572, but is still in compliance with EU Directive 2011/65/EU (RoHS 2).

**Notes:**

1. The Environment Friendly Use Period indicated by labelling on this product is applicable only to use under normal conditions.

2. Individual components including the CPU, RAM/memory, HDD, optical drive, and PSU are optional.
3. LCD Module and Touch Control Module only applies to certain products which feature these components.

# Table of Contents

---

<b>Chapter 1 - Product Specifications</b> .....	<b>1</b>
1.1 Specifications .....	2
<b>Chapter 2 – Hardware Information</b> .....	<b>5</b>
2.1 Dimensions .....	6
2.2 Jumpers and connectors .....	7
2.3 List of Jumpers .....	8
2.3.1 Setting Jumpers .....	8
2.3.2 Auto Power Button (JP5) .....	9
2.3.3 Clear CMOS (JP10) .....	9
2.4 List of Connectors .....	10
2.4.1 SATA PWR Port (CN3) .....	12
2.4.2 SATA Port (CN4) .....	13
2.4.3 Mini Card Connector (CN5/CN33) .....	13
2.4.4 SPI ROM connector for debugging (CN8) .....	14
2.4.5 COM port RS-232/422/485 BOX connector (CN9/CN12/CN14/CN18) .....	15
2.4.6 USB 3.0 (CN26, CN27) .....	16
2.4.7 COM port RS-232/422/485 (CN30/CN31/CN37) .....	17
2.4.8 Power Switch connector (internal BOX connector) (CN36) .....	17
2.4.9 DC-IN (CN38) .....	18
2.4.10 LPC Port (CN45) .....	18
2.4.11 USB2.0 connector (internal BOX connector) (CN53, CN54) .....	19
2.4.12 HDMI Port (CN61) .....	19
2.4.13 Remote switch connector (CN63) .....	20
2.4.14 VGA Port (CN64) .....	20
2.4.15 VGA port BOX connector (CN65) .....	21

2.5	Installing DRAM and mSATA modules .....	22
<b>Chapter 3 - AMI BIOS Setup .....</b>		<b>26</b>
3.1	System Test and Initialization.....	27
3.2	AMI BIOS Setup.....	28
3.3	Setup Submenu: Main .....	29
3.4	Setup Submenu: Advanced.....	30
3.4.1	Advanced: Trusted Computing .....	31
3.4.2	Advanced: CPU Configuration.....	33
3.4.3	Advanced: SATA Drives .....	36
3.4.4	Advanced: Hardware Monitor.....	37
3.4.5	Advanced: SIO Configuration .....	38
3.4.5.1	SIO Configuration: Serial Port 1 Configuration.....	39
3.4.5.2	SIO Configuration: Serial Port 2 Configuration.....	40
3.4.5.3	SIO Configuration: Serial Port 3 Configuration.....	41
3.4.6	Power Management .....	42
3.5	Setup submenu: Chipset .....	43
3.5.1	Chipset: North Bridge .....	44
3.5.2	Chipset: South Bridge.....	45
3.6	Setup submenu: Security .....	46
3.6.1	Secure Boot.....	47
3.6.2	Key Management .....	48
3.7	Setup submenu: Boot .....	52
3.8	Setup submenu: Save & Exit .....	53
<b>Chapter 4 – Drivers Installation.....</b>		<b>54</b>
4.1	Driver Download and Installation .....	55
<b>Appendix A - Watchdog Timer Programming .....</b>		<b>59</b>
A.1	Watchdog Timer Initial Program.....	60
A.2	Watchdog Sample Program.....	61

<b>Appendix B - I/O Information</b> .....	<b>65</b>
B.1 I/O Address Map .....	66
B.2 Memory Address Map .....	68
B.3 IRQ Mapping Chart .....	69
<b>Appendix C – Digital I/O Ports</b> .....	<b>70</b>
C.1 Electrical Specifications for Digital I/O Ports .....	71
C.2 DIO Programming .....	72
C.3 Digital I/O Register .....	73
C.4 Digital I/O Sample Program .....	74
<b>Appendix D – AI Core X</b> .....	<b>80</b>
D.1 AI Core X (PER-TAICX-A10) Manual .....	81

# Chapter 1

---

Product Specifications

## 1.1 Specifications

---

### System

CPU	Intel® Celeron™ N3350, Pentium™ N4200
Chipset	Intel® System on Chip
System Memory	DDR3L SO-DIMM slot x 1 Supports 1867 MHz and up to 8GB
AI Solution	Intel® Movidius™ Myriad™ X x1
Display Interface	HDMI 1.4 VGA
Storage Device	mSATA
Ethernet	10/100/1000 Base-TX x2
I/O	Power Button x 1 USB Type A x 4 for USB3.0 HDMI type A x 1 for HDMI v1.4b RJ45 x 2 for GbE LAN with LED indicator (i211-AT x2) Power Input x 1 3-pin terminal block in default (+, -, GND) Co-layout Mic-in x 1, Line-out x 1 DB-9 x 3 for RS-242/422/485 (Switch by BIOS) DB-15 x1 for VGA Remote On/Off Antenna Holes x 2 DC-in 3-pin terminal block(9~24V) x1



## System

Expansion	Half-size Minicard slot x 1 (mSATA only)
Indicator	Power LED x1 HDD active LED x1
OS Support	Windows® 10, Windows® 10 IoT Linux Debian 9.8

## Power Supply

Power Requirement	3 Pin 9-24V DC-in terminal block
-------------------	----------------------------------

## Mechanical

Mounting	Wallmount
Dimensions (W x H x D)	6.54" x 4.2" x 1.38" (166mm x 106.6mm x 35mm)
Gross Weight	3.6 lbs. (1.6kg)
Net Weight	1.76 lbs. (0.8 kg)

## Environmental

Operating Temperature	-13°F ~ 131°F (-25°C ~ 55°C) with W.T. SSD (according to IEC68-2-14 with 0.5 m/s airflow; with industrial devices)
Storage Temperature	-4°F ~ 158°F (-20°C ~ 70°C)
Storage Humidity	95% @ 40°C, non-condensing
Anti-Vibration	3 Grms/ 5 ~ 500Hz/ operation – mSATA
Certification	CE/FCC class A



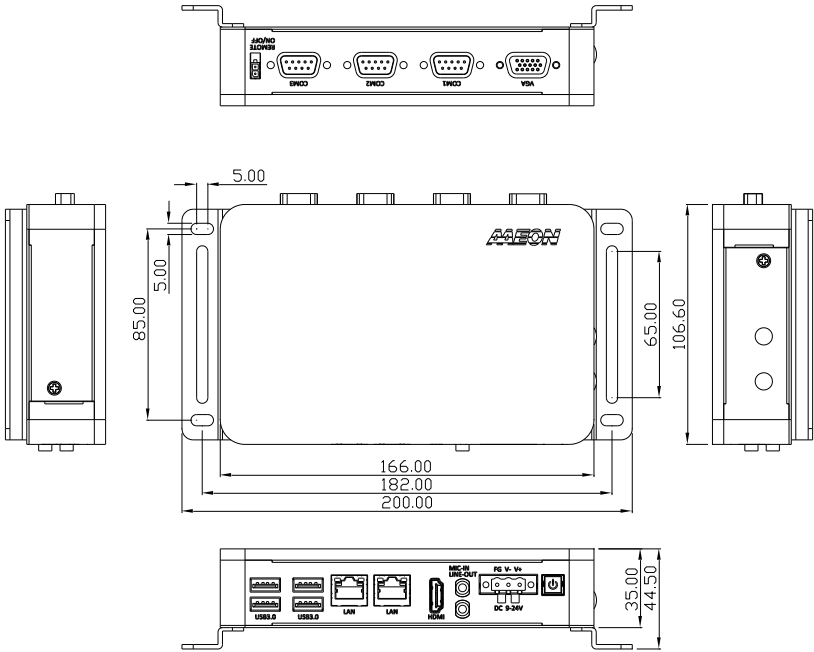
# Chapter 2

---

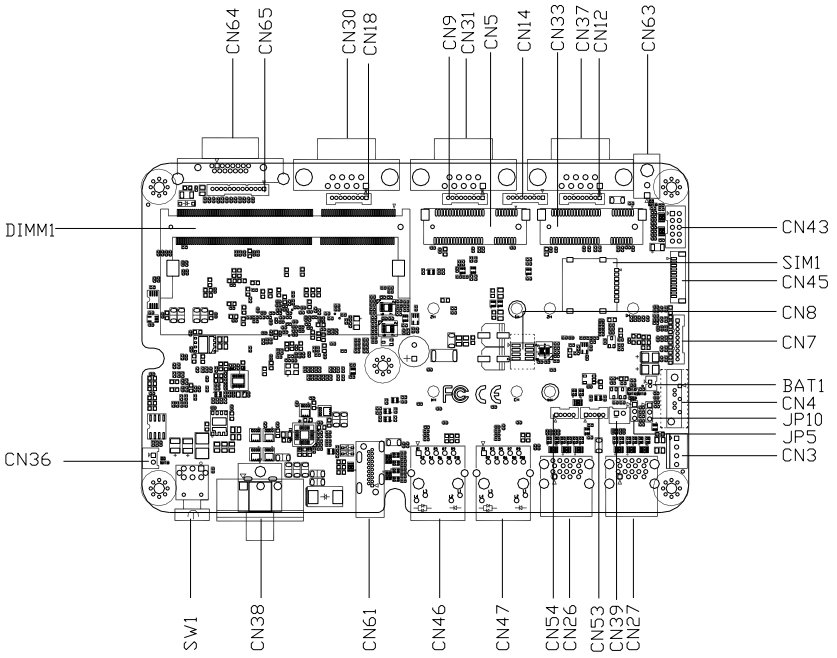
Hardware Information

## 2.1 Dimensions

### BOXER-8310AI



## 2.2 Jumpers and connectors



## 2.3 List of Jumpers

---

Please refer to the table below for all of the system's jumpers that you can configure for your application

Label	Function
JP5	AT/ATX mode select
JP10	Clear CMOS

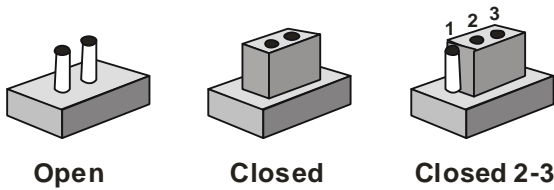
### 2.3.1 Setting Jumpers

---

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them.

To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



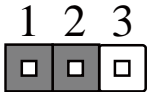
A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

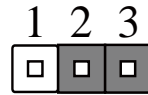
Generally, you simply need a standard cable to make most connections.

### 2.3.2 Auto Power Button (JP5)

---



Disable

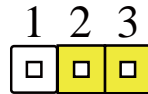
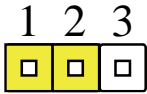


Enable (Default)

JP5	Function
1-2	ATX (Default)-
2-3	AT

### 2.3.3 Clear CMOS (JP10)

---



JP10	Function
1-2	Normal (Default)
2-3	Clear CMOS

## 2.4 List of Connectors

---

Please refer to the table below for all of the system's connectors that you can configure for your application

Label	Function
CN3	SATA PWR connector
CN4	SATA connector
CN5	Minicard connector
CN7	Audio Jack Connector (BOX connector)
CN8	SPI ROM connector
CN9	COM2 Port BOX connector (RS232/422/485)
CN12	COM3 Port BOX connector (RS232/422/485)
CN14	COM4 Port BOX connector (RS232/422/485)
CN18	COM1 Port BOX connector (RS232/422/485)
CN26	Dual stack USB (3.0/2.0)
CN27	Dual stack USB (3.0/2.0)
CN30	COM1 Port (RS232/422/485)
CN31	COM2 Port (RS232/422/485)
CN33	Minicard connector
CN36	Remote button cable connector (BOX connector)
CN37	COM3 Port (RS232/422/485)
CN38	DC-IN
CN39	SATA LED connector
CN43	DIO connector
CN45	Debug port connector
CN46	RJ-45 LAN connector
CN47	RJ-45 LAN connector
CN53	USB 2.0 Connector (BOX connector)



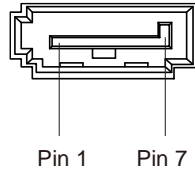
Label	Function
CN54	USB 2.0 Connector (BOX connector)
CN61	HDMI connector
CN63	Remote button connector
CN64	CRT port
CN65	CRT port (BOX connector)
BAT1	RTC battery connector
DIMM1	SO DIMM connector
SIM1	SIM1 card connector
SW1	Power button connector (BOX connector)

## 2.4.1 SATA PWR Port (CN3)

---

Pin	Pin Name	Level
1	+12V	12V
2	GND	GND
3	GND	GND
4	+5V	5V

## 2.4.2 SATA Port (CN4)



Pin	Pin Name	Signal Type	Signal Level
1	GND #	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

## 2.4.3 Mini Card Connector (CN5/CN33)

Pin	Signal	Pin	Signal
1	PCIE_WAKE#	2	+V3.3A
3	NC	4	GND
5	NC	6	+1.5V
7	PCIE_CLK_REQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	PCIE_REF_CLK-	12	UIM_CLK
13	PCIE_REF_CLK+	14	UIM_RST
15	GND	16	UIM_VPP
17	NC	18	GND

Pin	Signal	Pin	Signal
19	NC	20	W_DISABLE#
21	GND	22	PCIE_RST#
23	PCIE_RX-	24	+V3.3A
25	PCIE_RX+	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PCIE_TX-	32	SMB_DATA
33	PCIE_TX+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+V3.3A	40	GND
41	+V3.3A	42	NC
43	GND	44	NC
45	NC	46	NC
47	NC	48	+1.5V
49	NC	50	GND
51	NC	52	+V3.3A

#### 2.4.4 SPI ROM connector for debugging (CN8)

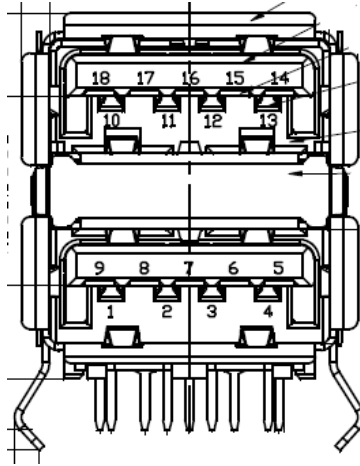
Pin	Signal	Pin	Signal
1	SPI_VCC	2	GND
3	SPI_CE	4	SPI_CLK
5	SPI_DATA_OUT	6	SPI_DATA_IN
7	NC	8	NC

## 2.4.5 COM port RS-232/422/485 BOX connector (CN9/CN12/CN14/CN18)

---

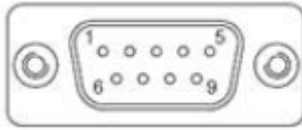
Pin	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	DSR	NC	NC
3	RXD	TX+	DATA+
4	RTS	NC	NC
5	TXD	RX+	NC
6	CTS	NC	NC
7	DTR	RX-	NC
8	RI	NC	NC
9	GND	NC	NC

## 2.4.6 USB 3.0 (CN26, CN27)



Pin	Signal	Pin	Signal
1	VBUS_1	2	VBUS_2
3	(A)D-	4	(B)D-
5	(A)D+	6	(B)D+
7	GND	8	GND
9	(A)SSRX-	10	(B)SSRX-
11	(A)SSRX+	12	(B)SSRX+
13	GND	14	GND
15	(A)SSTX-	16	(B)SSTX-
17	(A)SSTX+	18	(B)SSTX+

## 2.4.7 COM port RS-232/422/485 (CN30/CN31/CN37)



Pin	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	RXD	TX+	DATA+
3	TXD	RX+	NC
4	DTR	RX-	NC
5	GND	NC	NC
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

## 2.4.8 Power Switch connector (internal BOX connector) (CN36)

Pin	Signal	Pin	Signal
1	PANSWH#	2	GND-

### 2.4.9 DC-IN (CN38)

---

Pin	Signal	Pin	Signal
1	PWR_IN	2	GND
3	NC		

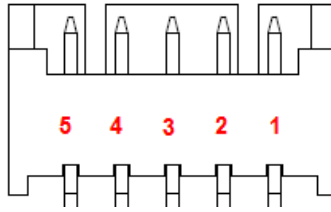
### 2.4.10 LPC Port (CN45)

---

Pin	Pin Name	Signal Type	Signal Level
1	LAD0	I/O	+3.3V
2	LAD1	I/O	+3.3V
3	LAD2	I/O	+3.3V
4	LAD3	I/O	+3.3V
5	+3.3V	PWR	+3.3V
6	LFRAME#	IN	
7	LRESET#	OUT	+3.3V
8	GND	GND	
9	LCLK	OUT	
10	I2C CLK	I/O	+3.3V
11	I2C DATA	I/O	+3.3V
12	SERIRQ	I/O	+3.3V



### 2.4.11 USB2.0 connector (internal BOX connector) (CN53, CN54)



Pin	Signal	Pin	Signal
1	VBUS	2	USB1-
3	USB+	4	GND
5	GND		

### 2.4.12 HDMI Port (CN61)

Pin	Signal	Pin	Signal
1	HDMI_DATA2_P	2	GND
3	HDMI_DATA2_N	4	HDMI_DATA1_P
5	GND	6	HDMI_DATA1_N
7	HDMI_DATA0_P	8	GND
9	HDMI_DATA0_N	10	HDMI_CLK_P
11	GND	12	HDMI_CLK_N
13	NC	14	NC
15	HDMI_SCL	16	HDMI_SDA
17	GND	18	HDMI_PWR
19	HDMI_HDP		

### 2.4.13 Remote switch connector (CN63)

---

Pin	Signal	Pin	Signal
1	PANSWH#	2	GND

---

### 2.4.14 VGA Port (CN64)

---

Pin	Signal	Pin	Signal
1	Red	2	Green
3	Blue	4	NC
5	GND	6	GND
7	GND	8	GND
9	VGA_VCC	10	GND
11	NC	12	DDC_DATA
13	HSYNC	14	VSYNC
15	DDC_CLK		

---

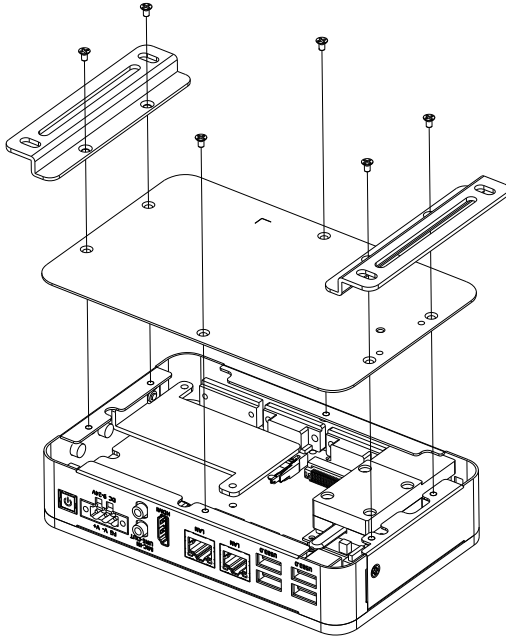
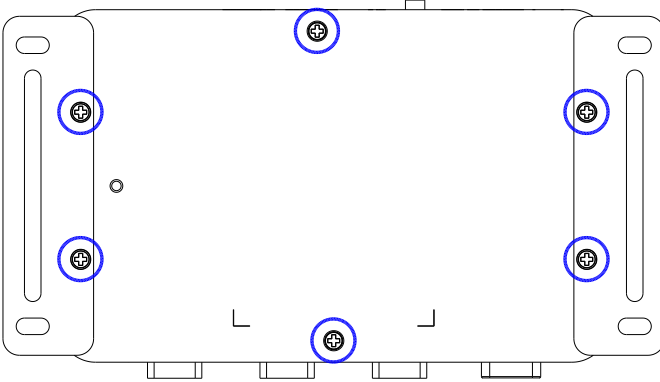
## 2.4.15 VGA port BOX connector (CN65)

---

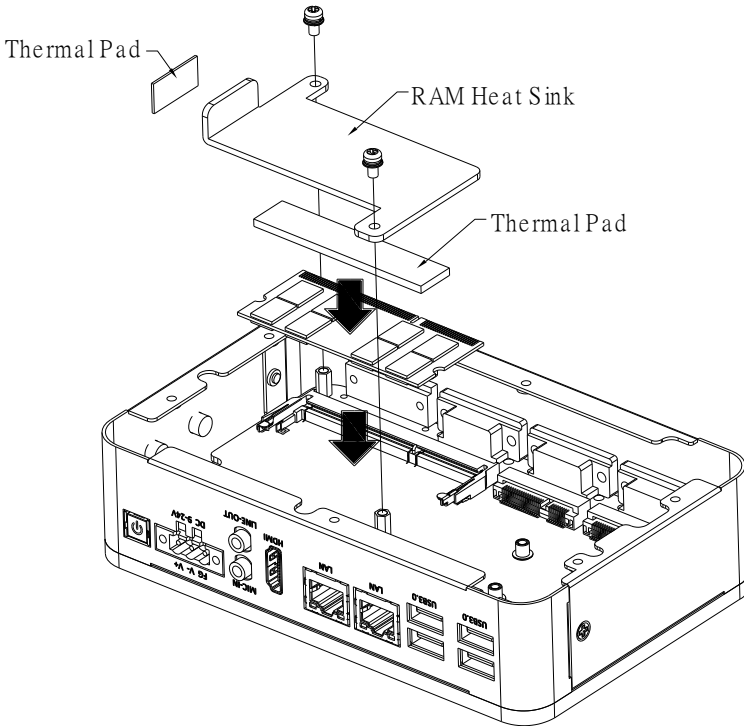
Pin	Signal	Pin	Signal
1	VSYNC	2	HSYNC
3	NC	4	DDC_CLK
5	DDC_DATA	6	GND
7	Blue	8	GND
9	Green	10	GND
11	Red	12	GND
13	VGA_VCC		

## 2.5 Installing DRAM and mSATA modules

1. Remove the screws as shown below; then remove the cover.



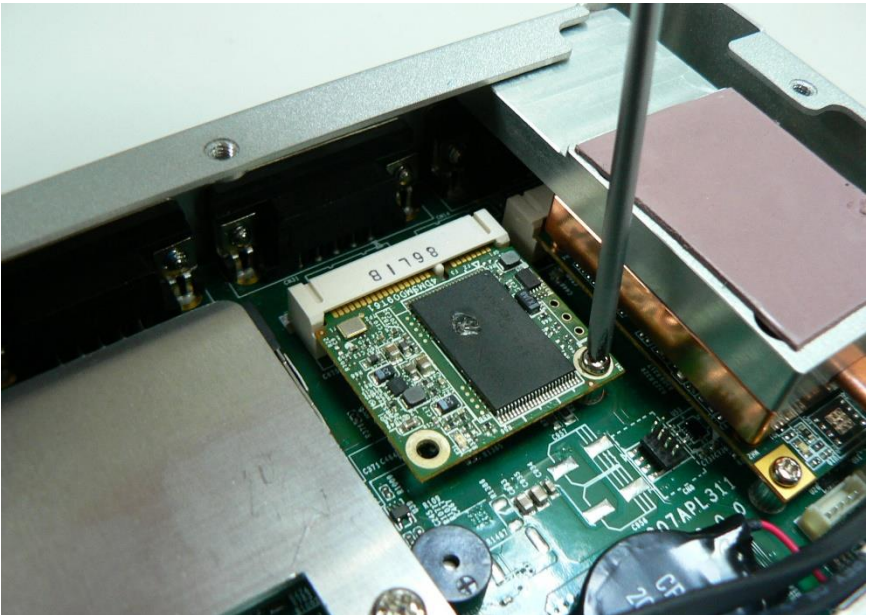
- To install RAM modules, insert the RAM at an angle and push down to secure. Place the thermal pads between the RAM module and RAM Heat Sink as well as between the RAM Heat Sink and chassis as shown below. Secure the assembly per the diagram below.



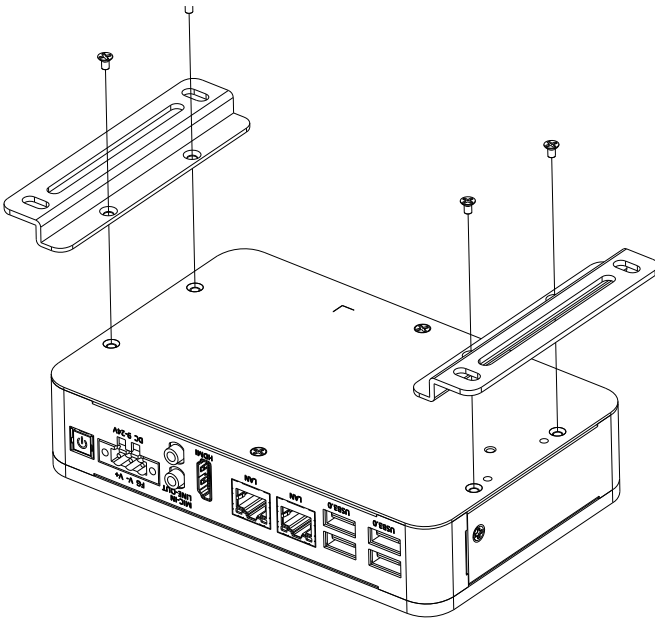
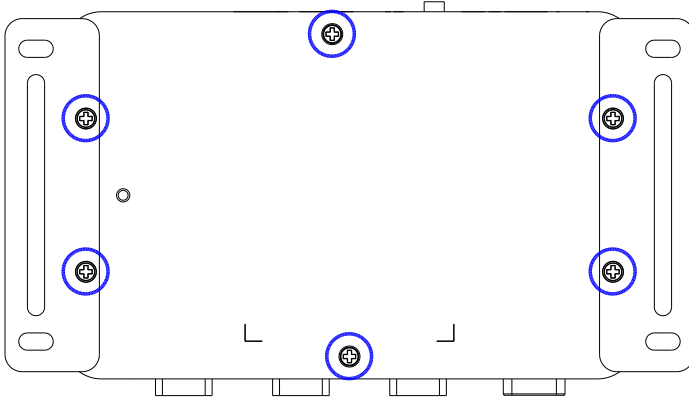
3. To install mSATA storage, insert mSATA device into slot at an angle as shown.



Push down and secure as in the picture below:



4. Re-tighten the screws.



# Chapter 3

---

AMI BIOS Setup



## 3.1 System Test and Initialization

---

The system uses certain routines to perform testing and initialization during the boot up sequence. If an error, fatal or non-fatal, is encountered, the system will output a few short beeps or an error message. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be output, and the BIOS setup program will need to be run to set the configuration information in memory.

There are three situations in which the CMOS settings will need to be set or changed:

- Starting the system for the first time
- The system hardware has been changed
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention. The battery must be replaced when it runs down.

## 3.2 AMI BIOS Setup

---

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

**Main** – Date and time can be set here. Press <Tab> to switch between date elements

**Advanced** – Enable/ disable boot option for legacy network devices

**Chipset** – For hosting bridge parameters

**Boot** – Enable/ disable Quiet Boot option

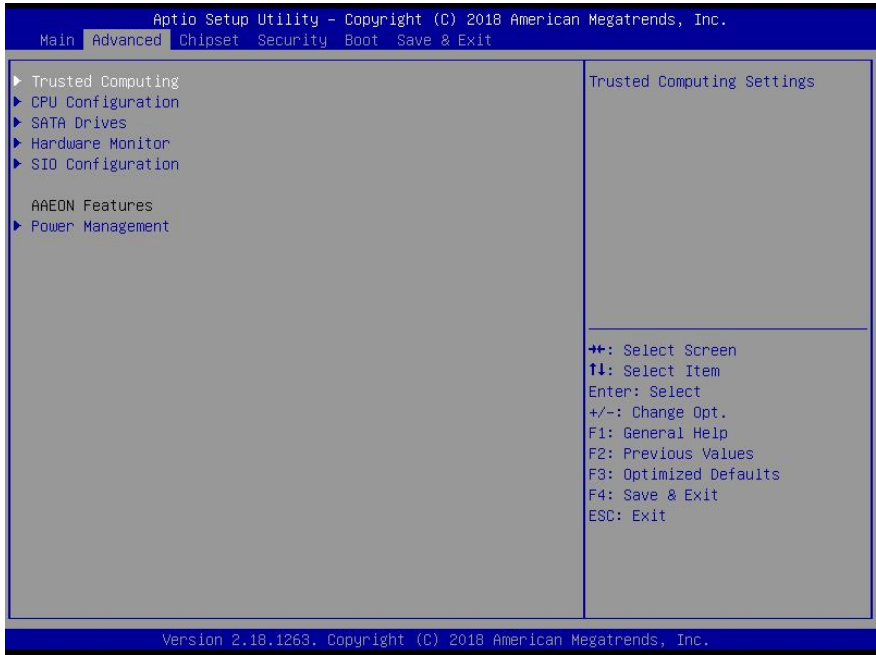
**Security** – The setup administrator password can be set here

**Save & Exit** – Save your changes and exit the program

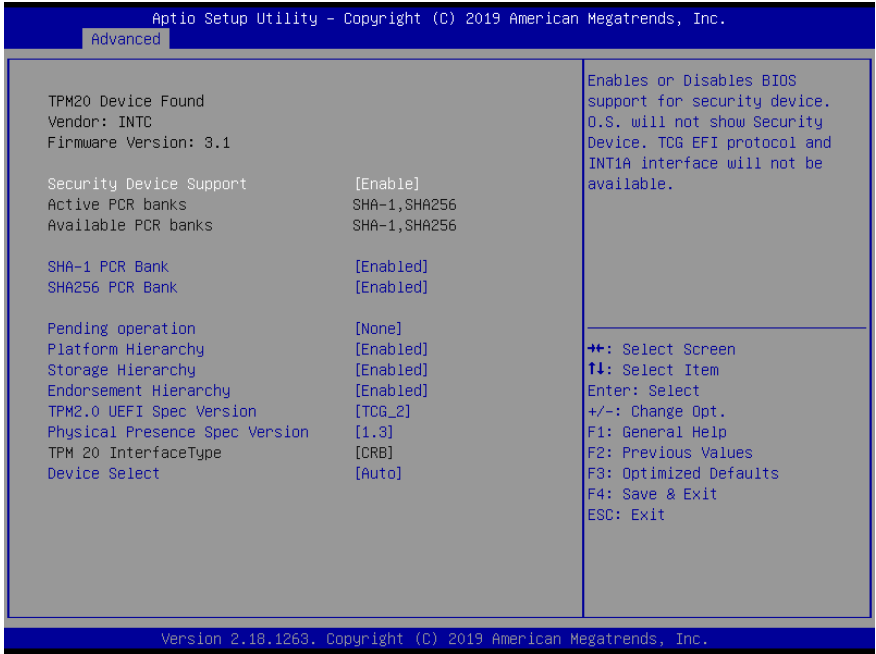
### 3.3 Setup Submenu: Main



### 3.4 Setup Submenu: Advanced



### 3.4.1 Advanced: Trusted Computing



Options Summary		
Security Device Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Security Device. NOTE: Your Computer will reboot during restart in order to change State of the Device.		
SHA-1 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SHA-1 PCR Bank		
SHA256 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SHA256 PCR Bank		
Pending Operation	TPM Clear	
	None	Optimal Default, Failsafe Default
Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.		

Options Summary		
<b>Platform Hierarchy</b>	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Platform Hierarchy		
<b>Storage Hierarchy</b>	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Storage Hierarchy		
<b>Endorsement Hierarchy</b>	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Endorsement Hierarchy		
<b>TPM2.0 UEFI Spec Version</b>	TCG_2	Optimal Default, Failsafe Default
	TCG_1_2	
Select the TCG2 Spec Version Support, TCG_1_2: the Compatible mode for Win8/Win10, TCG_2: Support new TCG2 protocol and event format for Win10 or later		
<b>Physical presence Spec Version</b>	1.3	Optimal Default, Failsafe Default
	1.2	
Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.		
<b>TPM 20 InterfaceType</b>	TIS	Optimal Default, Failsafe Default
	CRB	
Select the Communication Interface to TPM 20 Device.		
<b>Device Select</b>	Auto	Optimal Default, Failsafe Default
	TPM 1.2	
	TPM 2.0	
TPM 1.2 will restrict support to TPM 1.2 devices, TPM 2.0 will restrict support to TPM 2.0 devices, Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated		

### 3.4.2 Advanced: CPU Configuration

Aptio Setup Utility - Copyright (C) 2019 American Megatrends, Inc.

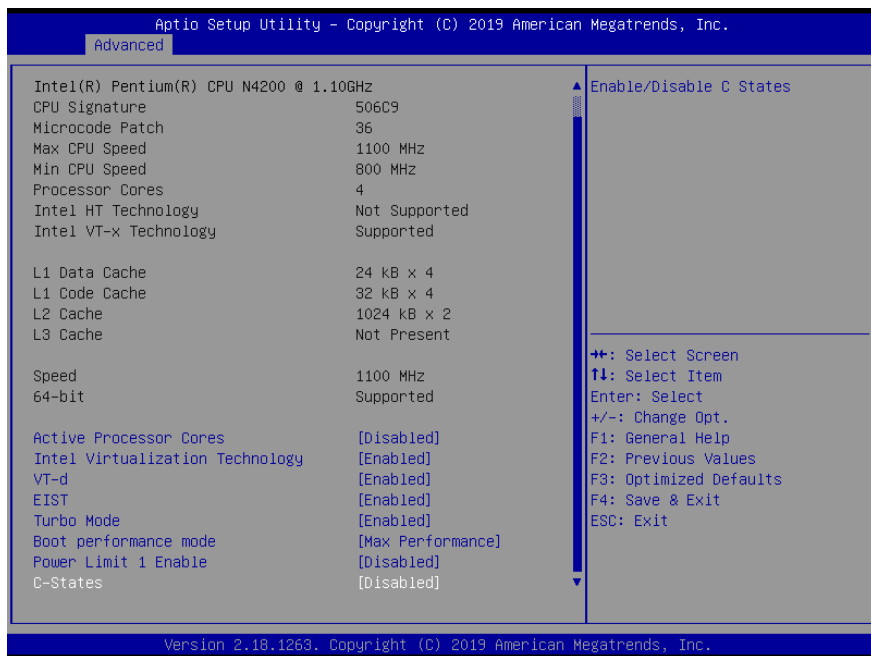
Advanced

CPU Configuration	
Intel(R) Pentium(R) CPU N4200 @ 1.10GHz	
CPU Signature	506C9
Microcode Patch	36
Max CPU Speed	1100 MHz
Min CPU Speed	800 MHz
Processor Cores	4
Intel HT Technology	Not Supported
Intel VT-x Technology	Supported
L1 Data Cache	24 kB x 4
L1 Code Cache	32 kB x 4
L2 Cache	1024 kB x 2
L3 Cache	Not Present
Speed	1100 MHz
64-bit	Supported
Active Processor Cores	[Disabled]
Intel Virtualization Technology	[Enabled]
VT-d	[Enabled]
EIST	[Enabled]
Turbo Mode	[Enabled]
Boot performance mode	[Max Performance]

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology

++: Select Screen  
↑↓: Select Item  
Enter: Select  
+/-: Change Opt.  
F1: General Help  
F2: Previous Values  
F3: Optimized Defaults  
F4: Save & Exit  
ESC: Exit

Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.



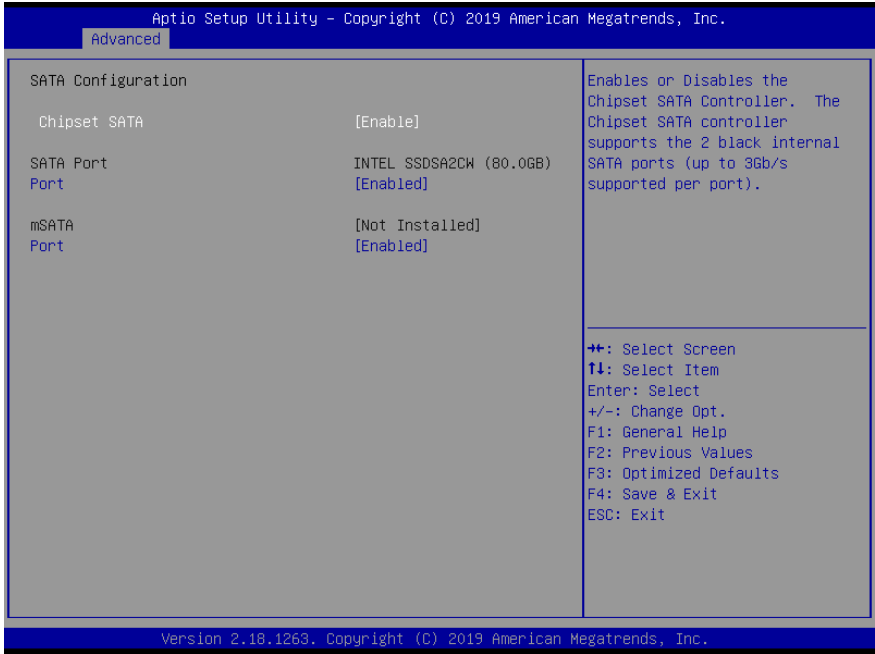
Options Summary		
Active Processor Cores	Disabled	Optimal Default, Failsafe Default
	Enabled	
Number of cores to enable in each processor package		
Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
VT-d	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable CPU VT-d		
EIST	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep		
Turbo Mode	Disabled	
	Enabled	Optimal Default, Failsafe Default
Turbo Mode		

Table continues on next page



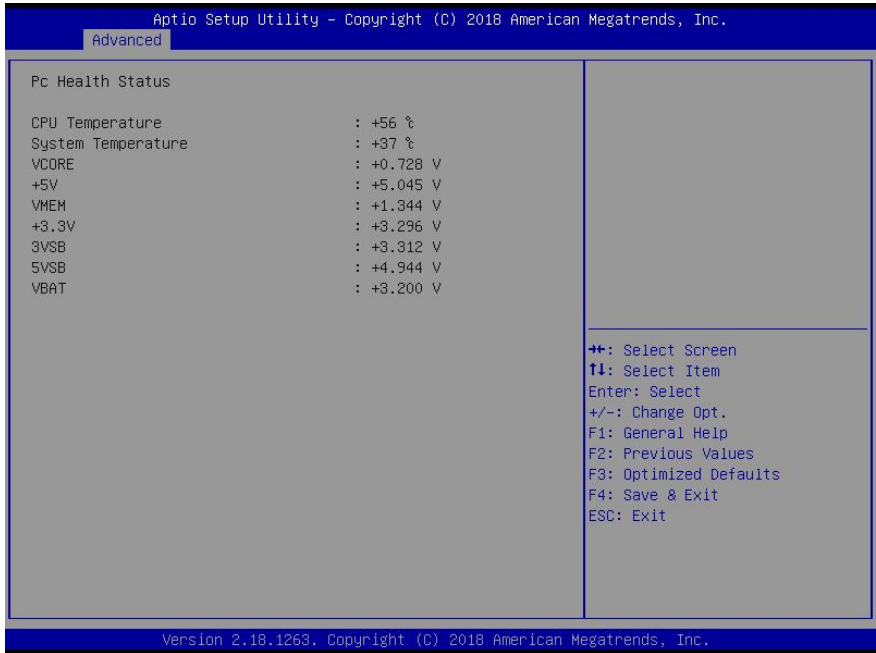
Options Summary		
<b>Boot performance mode</b>	Max performance	Optimal Default, Failsafe Default
	Max battery	
Select the performance state that the BIOS will set before OS handoff		
<b>Power Limit 1 Enable</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable Power Limit 1		
<b>C-States</b>	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable C States		

### 3.4.3 Advanced: SATA Drives

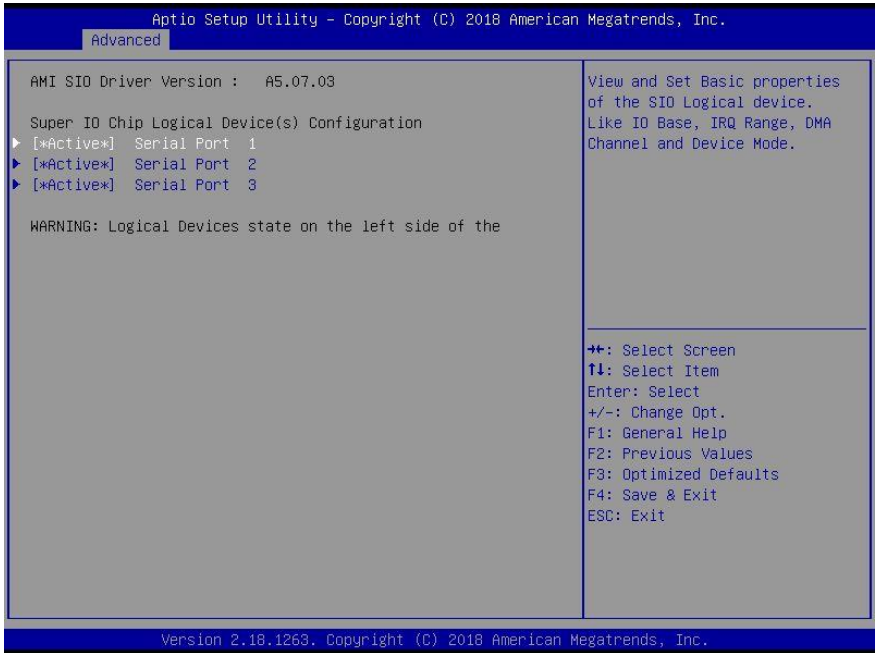


Options Summary		
Chipset SATA	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or Disable the Chipset SATA Controller. The Chipset SATA controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port)		
Port	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or Disable SATA Port		
Port	Enable	Optimal Default, Failsafe Default
	Disable	
Enable or Disable SATA Port		

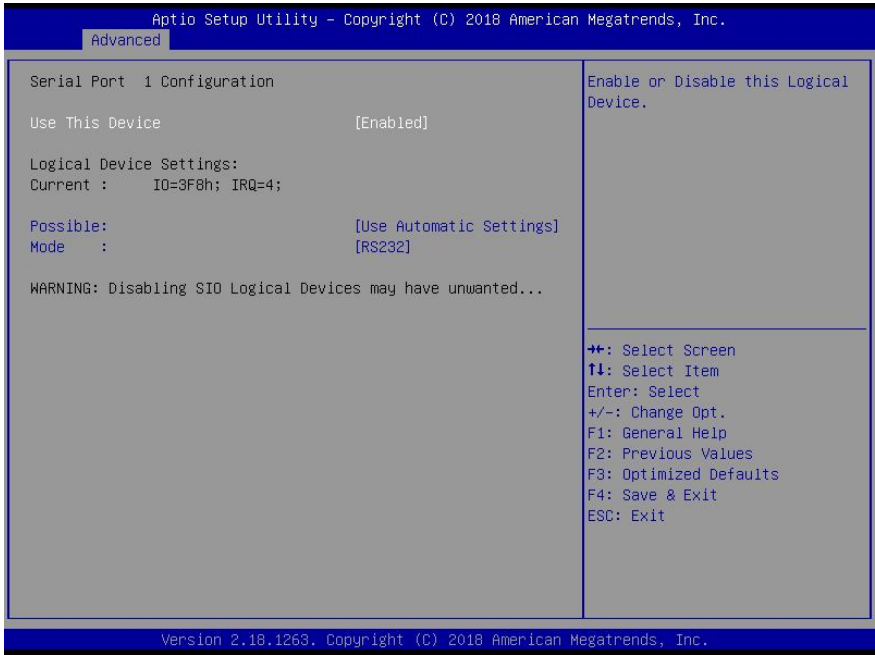
### 3.4.4 Advanced: Hardware Monitor



### 3.4.5 Advanced: SIO Configuration

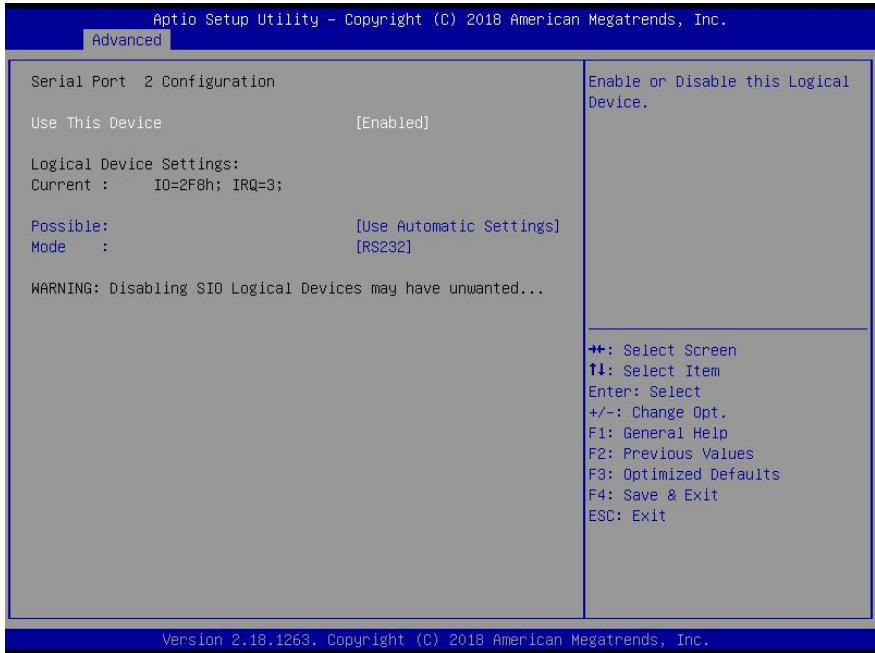


### 3.4.5.1 SIO Configuration: Serial Port 1 Configuration



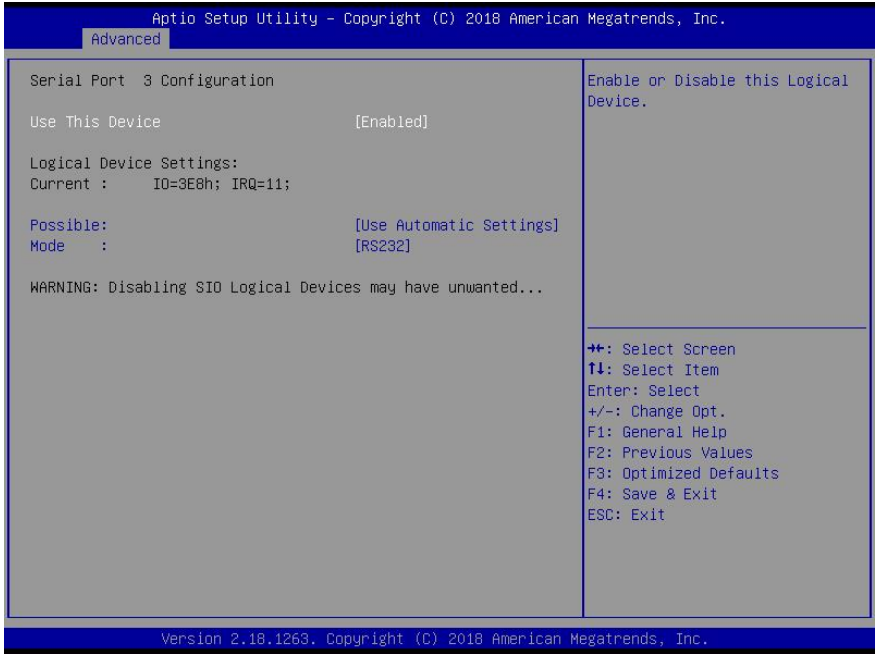
Options Summary		
Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4;	
	IO=2F8; IRQ=3;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS458	
UART RS232 RS422 RS485 selection		

### 3.4.5.2 SIO Configuration: Serial Port 2 Configuration



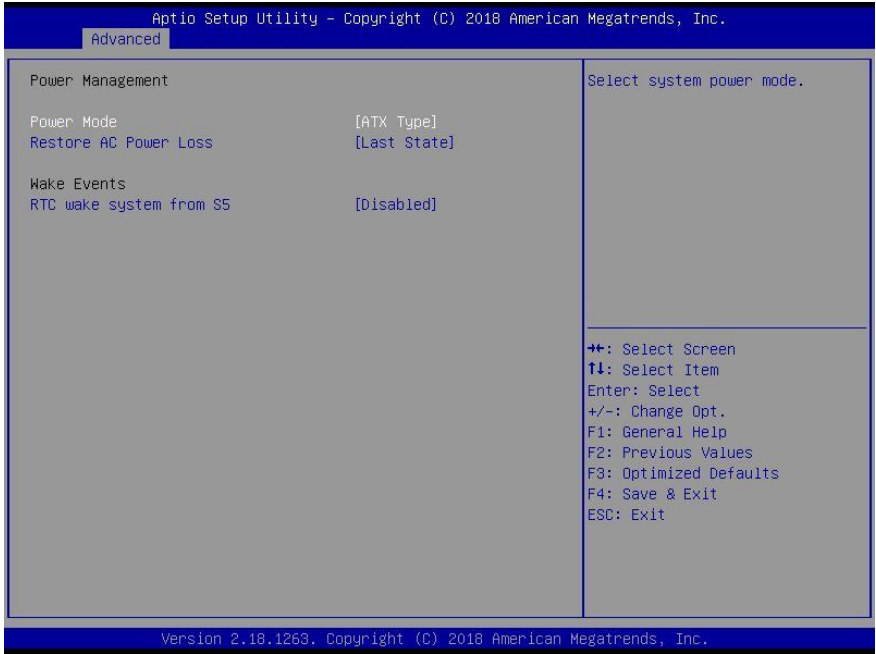
Options Summary		
Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS458	
UART RS232 RS422 RS485 selection		

### 3.4.5.3 SIO Configuration: Serial Port 3 Configuration



Options Summary		
Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable this Logical Device.		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8; IRQ=11;	
	IO=2E8; IRQ=11;	
Allows the user to change the device resource settings. New settings will be reflected on this setup page after system restarts.		
Mode:	RS232	Optimal Default, Failsafe Default
	RS422	
	RS458	
UART RS232 RS422 RS485 selection		

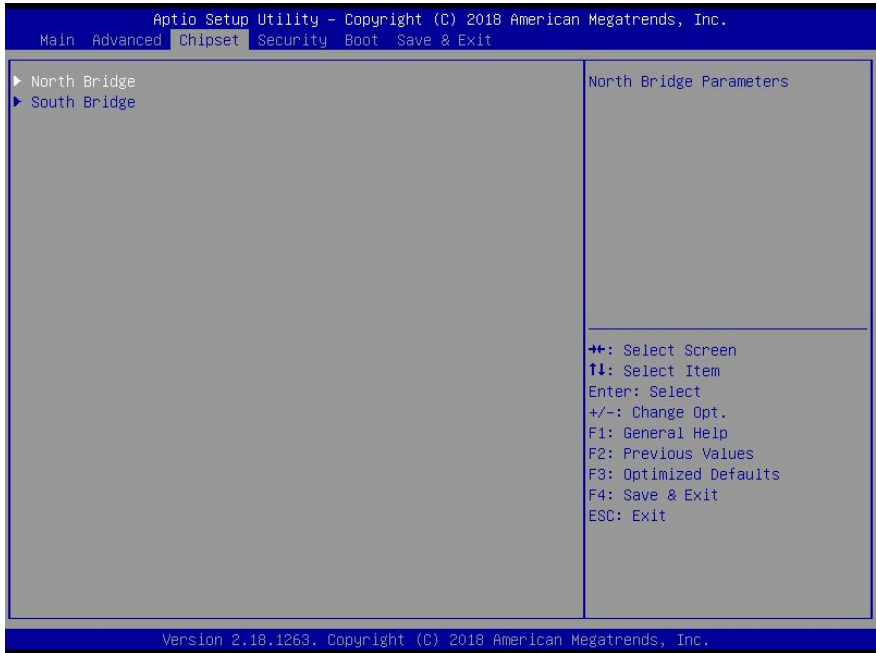
### 3.4.6 Power Management



Options Summary		
Power Mode	ATX Type	Optimal Default, Failsafe Default
	AT Type	
Select system power mode.		
Restore AC Power Loss	Last State	Optimal Default, Failsafe Default
	Power On	
	Power Loss	
RTC wake system from S5	Disabled	Optimal Default, Failsafe Default
	Fixed Time	
	Dynamic Time	
Enable or disable System wake on alarm event. When enabled, System will wake on the hr::min::sec specified		



### 3.5 Setup submenu: Chipset

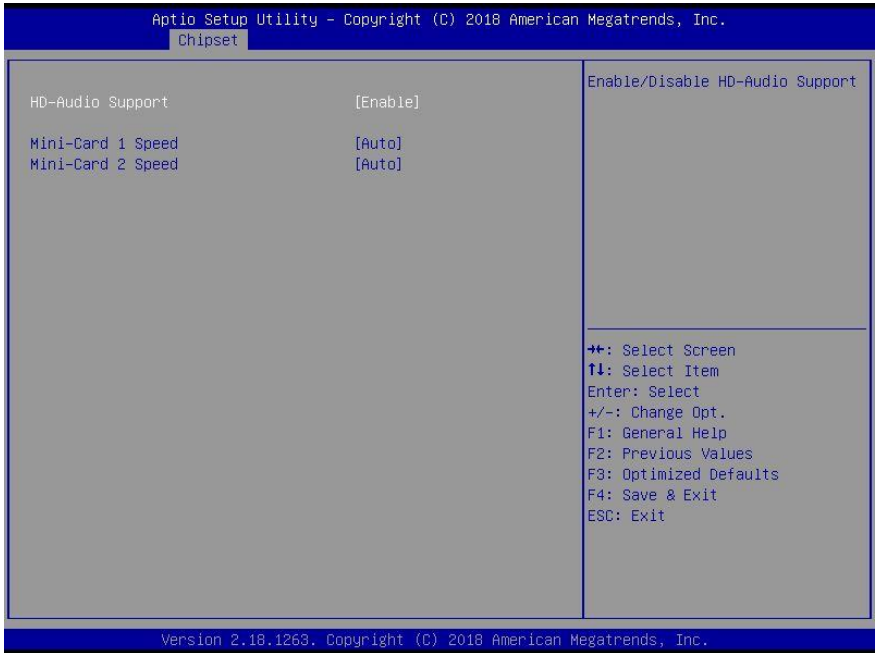


### 3.5.1 Chipset: North Bridge



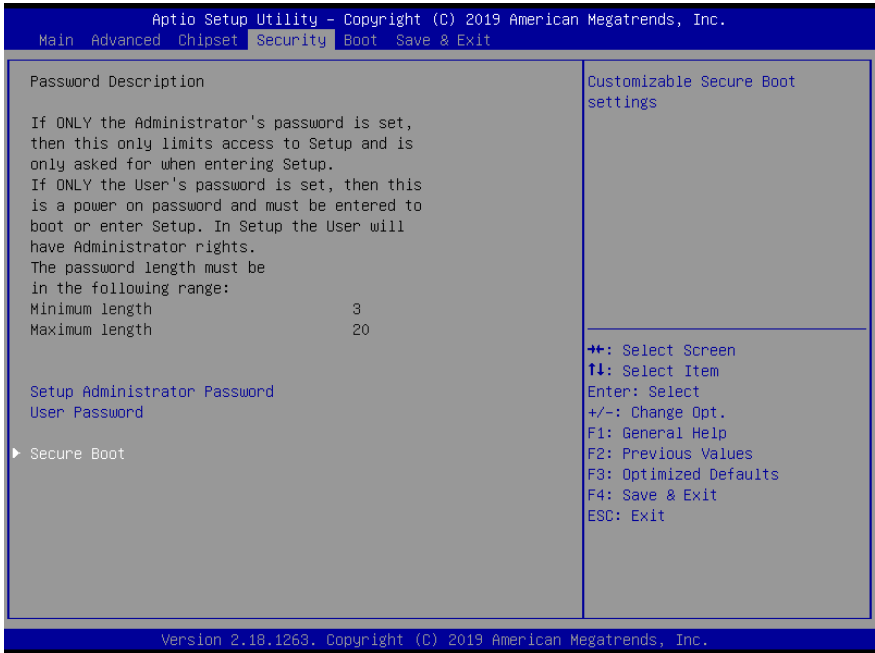
Options Summary		
DCMT Total Gfx Mem	128M	Optimal Default, Failsafe Default
	256M	
	MAX	
Select DVMT5.0 Total Graphics Memory size used by the Internal Graphics Device		

### 3.5.2 Chipset: South Bridge



Options Summary		
HD-Audio Support	Disable	Optimal Default, Failsafe Default
	Enable	
Enable/Disable HD-Audio Support		
Mini-Card 1 Speed	Auto	Optimal Default, Failsafe Default
	Gen 1	
	Gen 2	
Configure PCIe Speed		
Mini-Card 2 Speed	Auto	Optimal Default, Failsafe Default
	Gen 1	
	Gen 2	
Configure PCIe Speed		

## 3.6 Setup submenu: Security



### Change User/Administrator Password

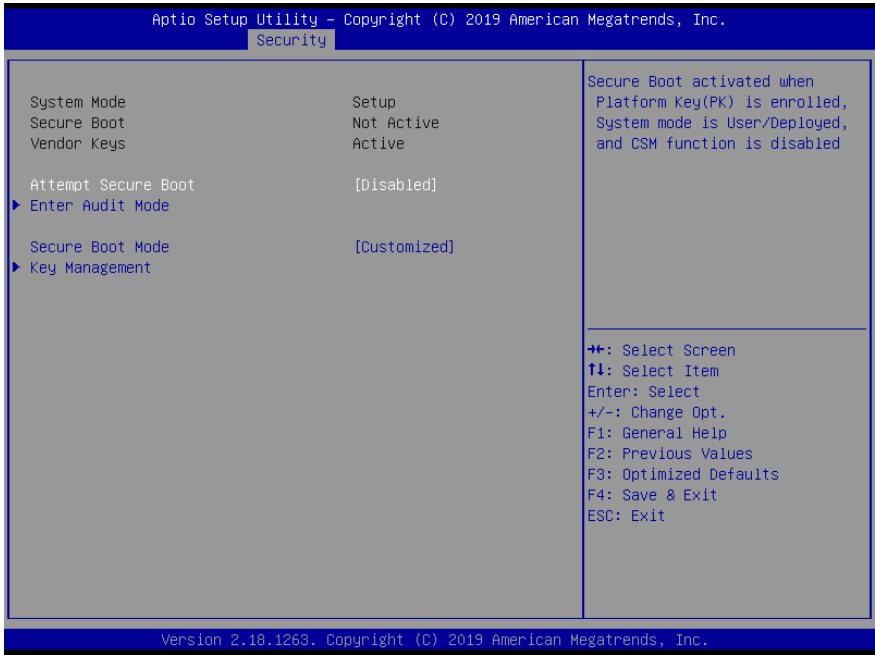
You can set an Administrator Password or User Password. An Administrator Password must be set before you can set a User Password. The password will be required during boot up, or when the user enters the Setup utility. A User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, and press Enter. In the dialog box, enter your password (must be between 3 and 20 letters or numbers). Press Enter and retype your password to confirm. Press Enter again to set the password.

### Removing the Password

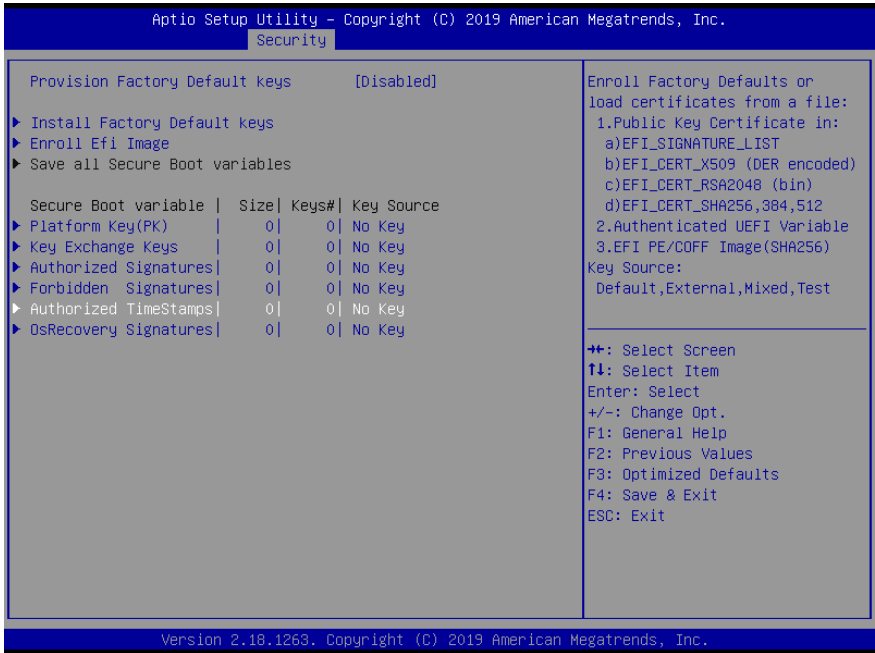
Select the password you want to remove and enter the current password. At the next dialog box press Enter to disable password protection.

### 3.6.1 Secure Boot



Options Summary		
<b>Attempt Secure Boot</b>	Disable	Optimal Default, Failsafe Default
	Enable	
Secure Boot activated when Platform key(PK) is enrolled, System mode is User/Deployed, and CSM function is disabled		
<b>Enter Audit Mode</b>	Enter Audit Mode. If current System Mode is User – PK variable will be erased on transition to Audit.	
<b>Secure Boot Mode</b>	Standard	Optimal Default, Failsafe Default
	Customized	
Secure Boot Mode – Customized & Standard, Set UEFI Secure Boot Mode to STANDARD mode or CUSTOMIZED mode. Changes go into effect after saving. Mode defaults to STANDARD if the system is reset.		
<b>Key Management</b>		
Enables expert users to modify Secure Boot Policy variables without full authentication		

## 3.6.2 Key Management



Options Summary		
Provision Factory Default keys	Disable	Optimal Default, Failsafe Default
	Enable	
Allow to provision factory default Secure Boot keys when System is in Setup Mode		
Install Factory Default Keys	No	Press 'Yes' to install factory default keys
	Yes	
Force System to User Mode – install all Factory Default keys		

Enroll Efi Image Settings		
Enroll Efi Image	Acpi(a0341d0, 0)\PCI(12 0)\DevicePath(Type 3, SubType 18)HD(Part1, Sig )\	\$AttrDef \$BadClus \$Bitmap \$Boot \$LogFile \$MFT \$MFTMirr \$Secure \$UpCase \$Volume <System Volume Information> <Recovery> <.> <\$Extend>
	Acpi(a0341d0, 0)\PCI(12 0)\DevicePath(Type 3, SubType 18)HD(Part2, Sig )\	<EFI>

## Enroll Efi Image Settings

	Acpi(a0341d0, 0)\PCI(12 0)\DevicePath(Type 3, SubType 18)HD(Part4, Sig )\	\$AttrDef \$BadClus \$Bitmap \$Boot \$LogFile \$MFT \$MFTMirr \$Secure \$UpCase \$Volume bootmgr BOOTNXT hiberfil.sys pagefile.sys swapfile.sys <Windows.old> <Windows> <Users> <System Volume Information> <Recovery> <ProgramData> <Program Files (x86)> <Program Files> <PerfLogs> <Intel> <Document and Settings> <.> <\$Recycle.Bin> <\$Extend>
--	---	--

Allow the image to run in Secure Boot mode.  
 Enroll SHA256 Hash Certificate of the Image into Authorized Signature Database (db)



## Secure Boot Variable

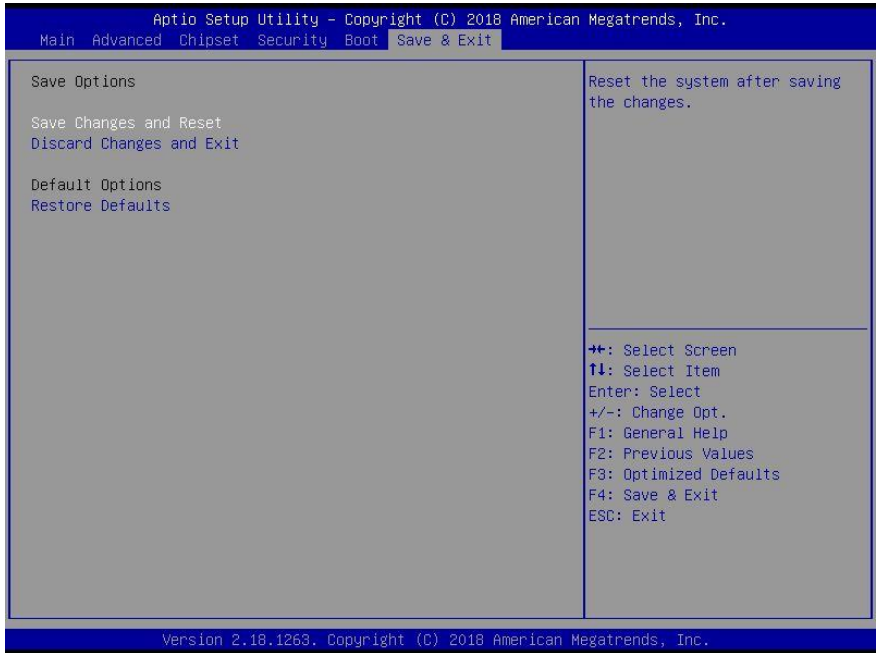
Secure Boot Variable Settings			
Platform key(PK)	Set New Var	No	Press 'Yes' to load factory default 'PK' or Select 'No' to load it from a file on external media
		Yes	
Key Exchange keys	Set New Var	No	Press 'Yes' to load factory default 'KEK' or Select 'No' to load it from a file on external media
		Yes	
	Append Key	No	Press 'Yes' to load factory default 'KEK' or Select 'No' to load it from a file on external media
		Yes	
Authorized Signatures	Set New Var	No	Press 'Yes' to load factory default 'db' or Select 'No' to load it from a file on external media
		Yes	
	Append Key	No	Press 'Yes' to load factory default 'db' or Select 'No' to load it from a File on external media
		Yes	
Forbidden Signatures	Set New Var	No	Press 'Yes' to load factory default 'dbx' or Select 'No' to load it from a file on external media
		Yes	
	Append Key	No	Press 'Yes' to load factory default 'dbx' or Select 'No' to load it from a file on external media
		Yes	
Authorized TimeStamps	Set New Var	No	Press 'Yes' to load factory default 'dbt' or Select 'No' to load it from a file on external media
		Yes	
	Append Key	No	Press 'Yes' to load factory default 'dbt' or Select 'No' to load it from a file on external media
		Yes	
OsRecovery Signatures	Set New Var	No	Press 'Yes' to load factory default 'dbr' or Select 'No' to load it from a file on external media
		Yes	
	Append Key	No	Press 'Yes' to load factory default 'dbr' or Select 'No' to load it from a file on external media
		Yes	

### 3.7 Setup submenu: Boot



Options Summary		
Quiet Boot	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable or Disable Quiet Boot option		
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Network Stack		

### 3.8 Setup submenu: Save & Exit



# Chapter 4

---

Drivers Installation

## 4.1 Driver Download and Installation

---

Drivers for the BOXER-8310AI can be downloaded from the product page on the AAEON website by following this link:

<https://www.aaeon.com/en/p/ai-edge-computing-fanless-box-pc-boxer-8310ai>

Download the driver(s) you need and follow the steps below to install them.

### Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder and select your OS
2. Open the **SetupChipset.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 2 – Install Graphics Driver

1. Open the **Step 2 - Graphics** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 3 – Install LAN Driver

1. Open the **Step 3 - LAN** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

#### Step 4 – Install USB 3.0 Drivers (Windows 7 only)

1. Open the **Step 4 – USB 3.0** followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

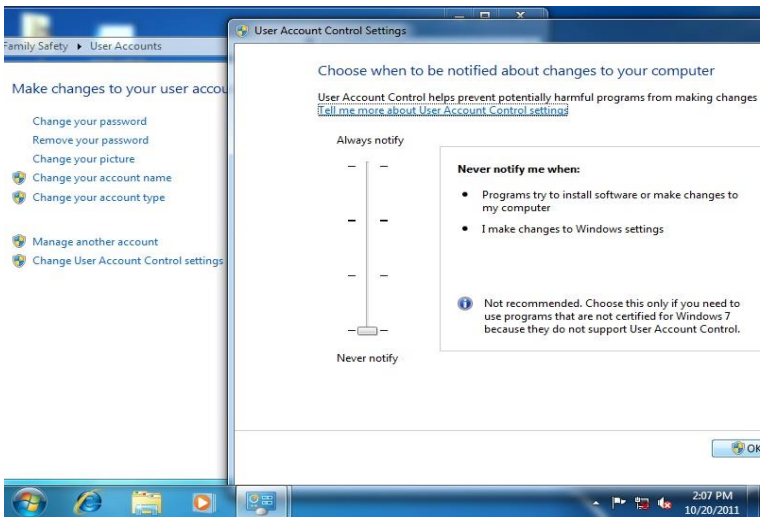
#### Step 5 – Install MBI Drivers

1. Open the **Step 5 – MBI(Optional)** folder and select your OS
2. Open the **Setup.exe** file
3. Follow the instructions
4. Drivers will be installed automatically

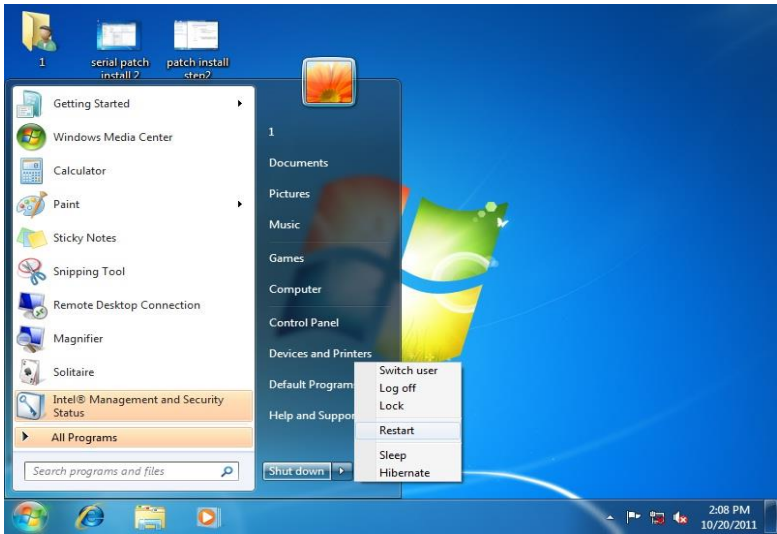
#### Step 6 – Install Serial Port Driver (Optional)

For Windows 7:

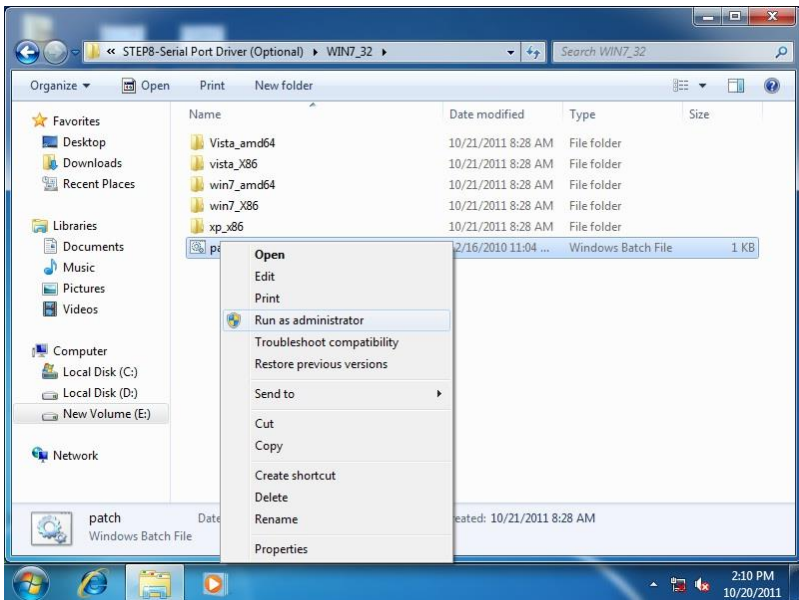
1. Change User Account Control settings to **Never notify**



2. Reboot and log in as administrator



3. Open the **Step 6 - Serial Port Driver (Optional)** folder and run **patch.bat** as administrator



### For Windows 8 and Windows 10:

1. Open the **Step 6 - Serial Port Driver (Optional)** folder and select your OS
2. Open the **batch.bat** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically



# Appendix A

---

## Watchdog Timer Programming

## A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

## A.2 Watchdog Sample Program

---

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte TimerLDN //This parameter is represented from Note3
#define byte TimerReg //This parameter is represented from Note4
#define byte TimerVal // This parameter is represented from Note24
#define byte UnitLDN //This parameter is represented from Note5
#define byte UnitReg //This parameter is represented from Note6
#define byte UnitBit //This parameter is represented from Note7
#define byte UnitVal //This parameter is represented from Note8
#define byte EnableLDN //This parameter is represented from Note9
#define byte EnableReg //This parameter is represented from Note10
#define byte EnableBit //This parameter is represented from Note11
#define byte EnableVal //This parameter is represented from Note12
#define byte StatusLDN // This parameter is represented from Note13
#define byte StatusReg // This parameter is represented from Note14
#define byte StatusBit // This parameter is represented from Note15
#define byte ModeLDN // This parameter is represented from Note16
#define byte ModeReg // This parameter is represented from Note17
#define byte ModeBit // This parameter is represented from Note18
#define byte ModeVal // This parameter is represented from Note19
#define byte WDTRstLDN // This parameter is represented from Note20
#define byte WDTRstReg // This parameter is represented from Note21
#define byte WDTRstBit // This parameter is represented from Note22
#define byte WDTRstVal // This parameter is represented from Note23
*****
```

```
*****
VOID Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```

```

*****
// Procedure : AaeonWDTEnable
VOID AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModelLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```

*****
VOID  SIOEnterMBPnPMode0{
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```

# Appendix B

---

I/O Information

## B.1 I/O Address Map

Input/output (IO)	
[0000000000000000 - 000000000000006F]	PCI Express Root Complex
[0000000000000020 - 0000000000000021]	Programmable interrupt controller
[0000000000000024 - 0000000000000025]	Programmable interrupt controller
[0000000000000028 - 0000000000000029]	Programmable interrupt controller
[000000000000002C - 000000000000002D]	Programmable interrupt controller
[000000000000002E - 000000000000002F]	Motherboard resources
[0000000000000030 - 0000000000000031]	Programmable interrupt controller
[0000000000000034 - 0000000000000035]	Programmable interrupt controller
[0000000000000038 - 0000000000000039]	Programmable interrupt controller
[000000000000003C - 000000000000003D]	Programmable interrupt controller
[0000000000000040 - 0000000000000043]	System timer
[000000000000004E - 000000000000004F]	Motherboard resources
[0000000000000050 - 0000000000000053]	System timer
[0000000000000061 - 0000000000000061]	Motherboard resources
[0000000000000063 - 0000000000000063]	Motherboard resources
[0000000000000065 - 0000000000000065]	Motherboard resources
[0000000000000067 - 0000000000000067]	Motherboard resources
[0000000000000070 - 0000000000000070]	Motherboard resources
[0000000000000070 - 0000000000000077]	System CMOS/real time clock
[0000000000000078 - 00000000000000CF7]	PCI Express Root Complex
[0000000000000080 - 000000000000008F]	Motherboard resources
[0000000000000092 - 0000000000000092]	Motherboard resources
[00000000000000A0 - 00000000000000A1]	Programmable interrupt controller
[00000000000000A4 - 00000000000000A5]	Programmable interrupt controller
[00000000000000A8 - 00000000000000A9]	Programmable interrupt controller
[00000000000000AC - 00000000000000AD]	Programmable interrupt controller
[00000000000000B0 - 00000000000000B1]	Programmable interrupt controller
[00000000000000B2 - 00000000000000B3]	Motherboard resources
[00000000000000B4 - 00000000000000B5]	Programmable interrupt controller
[00000000000000B8 - 00000000000000B9]	Programmable interrupt controller
[00000000000000BC - 00000000000000BD]	Programmable interrupt controller
[00000000000002F8 - 00000000000002FF]	Communications Port (COM2)
[00000000000003E8 - 00000000000003EF]	Communications Port (COM3)
[00000000000003F8 - 00000000000003FF]	Communications Port (COM1)
[0000000000000400 - 000000000000047F]	Motherboard resources
[00000000000004D0 - 00000000000004D1]	Programmable interrupt controller
[0000000000000500 - 00000000000005FE]	Motherboard resources
[0000000000000680 - 000000000000069F]	Motherboard resources
[0000000000000A00 - 0000000000000A0F]	Motherboard resources
[0000000000000A10 - 0000000000000A1F]	Motherboard resources



[000000000000A10 - 000000000000A1F] Motherboard resources  
[000000000000A20 - 000000000000A2F] Motherboard resources  
[000000000000D00 - 000000000000FFFF] PCI Express Root Complex  
[000000000000D000 - 000000000000DFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9  
[000000000000E000 - 000000000000EFFF] Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8  
[000000000000F000 - 000000000000F03F] Intel(R) HD Graphics  
[000000000000F040 - 000000000000F05F] Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4  
[000000000000F060 - 000000000000F07F] Standard SATA AHCI Controller  
[000000000000F080 - 000000000000F083] Standard SATA AHCI Controller  
[000000000000F090 - 000000000000F097] Standard SATA AHCI Controller

## B.2 Memory Address Map











Compact AI@Edge Box PC

BOXER-9310A1

Memory	
[000000007B800001 - 000000007BFFFFFF]	PCI Express Root Complex
[000000007C000001 - 000000007FFFFFFF]	PCI Express Root Complex
[0000000080000000 - 000000008FFFFFFF]	Intel(R) HD Graphics
[0000000080000000 - 00000000CFFFFFFF]	PCI Express Root Complex
[0000000090000000 - 0000000090FFFFFF]	Intel(R) HD Graphics
[0000000091000000 - 00000000910FFFFFFF]	High Definition Audio Controller
[0000000091100000 - 00000000911FFFFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD9
[00000000911DC000 - 00000000911DFFFFF]	Intel(R) I211 Gigabit Network Connection #2
[00000000911E0000 - 00000000911FFFFFFF]	Intel(R) I211 Gigabit Network Connection #2
[0000000091200000 - 00000000912FFFFFFF]	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD8
[00000000912DC000 - 00000000912DFFFFF]	Intel(R) I211 Gigabit Network Connection
[00000000912E0000 - 00000000912FFFFFFF]	Intel(R) I211 Gigabit Network Connection
[0000000091300000 - 000000009130FFFFFF]	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
[0000000091310000 - 0000000091313FFFFF]	High Definition Audio Controller
[0000000091314000 - 0000000091315FFFFF]	Standard SATA AHCI Controller
[0000000091318000 - 00000000913180FFFF]	Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
[0000000091319000 - 00000000913197FFFF]	Standard SATA AHCI Controller
[000000009131A000 - 000000009131A0FFFF]	Standard SATA AHCI Controller
[000000009131E000 - 000000009131EFFFFF]	Intel(R) Trusted Execution Engine Interface
[00000000D0C00000 - 00000000D0C00653]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C40000 - 00000000D0C40763]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C50000 - 00000000D0C5076B]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000D0C70000 - 00000000D0C70673]	Intel(R) Serial IO GPIO Host Controller - INT3452
[00000000E0000000 - 00000000EFFFFFFF]	Motherboard resources
[00000000E0000000 - 00000000EFFFFFFF]	PCI Express Root Complex
[00000000FEA00000 - 00000000FEAFFFFFFF]	Motherboard resources
[00000000FED00000 - 00000000FED003FF]	High precision event timer
[00000000FED01000 - 00000000FED01FFF]	Motherboard resources
[00000000FED03000 - 00000000FED03FFF]	Motherboard resources
[00000000FED06000 - 00000000FED06FFF]	Motherboard resources
[00000000FED08000 - 00000000FED09FFF]	Motherboard resources
[00000000FED1C000 - 00000000FED1CFFF]	Motherboard resources
[00000000FED40000 - 00000000FED44FFF]	Trusted Platform Module 2.0
[00000000FED80000 - 00000000FEDBFFFF]	Motherboard resources
[00000000FEE00000 - 00000000FEEFFFFFFF]	Motherboard resources

## B.3 IRQ Mapping Chart

---

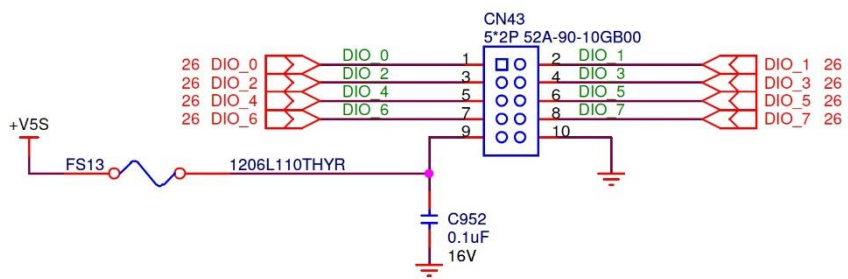
- ▼  Interrupt request (IRQ)
  -  (ISA) 0x00000000 (00) System timer
  -  (ISA) 0x00000003 (03) Communications Port (COM2)
  -  (ISA) 0x00000004 (04) Communications Port (COM1)
  -  (ISA) 0x00000008 (08) High precision event timer
  -  (ISA) 0x0000000B (11) Communications Port (COM3)
  -  (ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452
  -  (ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452
  -  (ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452
  -  (ISA) 0x0000000E (14) Intel(R) Serial IO GPIO Host Controller - INT3452

# Appendix C

---

Digital I/O Ports

## C.1 Electrical Specifications for Digital I/O Ports



GPIO50	DIO_0
GPIO51	DIO_1
GPIO52	DIO_2
GPIO53	DIO_3
GPIO54	DIO_4
GPIO55	DIO_5
GPIO56	DIO_6
GPIO57	DIO_7

## C.2 DIO Programming

---

The BOXER-8310AI utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

- (1) Enter the MB PnP Mode
- (2) Modify the data of configuration registers
- (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

### C.3 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0xA2(Note4)	0(Note5)		GPIO50
DIO-2 Pin Status	0x06(Note6)	0xA2(Note7)	1(Note8)		GPIO51
DIO-3 Pin Status	0x06(Note9)	0xA2(Note10)	2(Note11)		GPIO52
DIO-4 Pin Status	0x06(Note12)	0xA2(Note13)	3(Note14)		GPIO53
DIO-5 Pin Status	0x06(Note15)	0xA2(Note16)	4(Note17)		GPIO54
DIO-6 Pin Status	0x06(Note18)	0xA2(Note19)	5(Note20)		GPIO55
DIO-7 Pin Status	0x06(Note21)	0xA2(Note22)	6(Note23)		GPIO56
DIO-8 Pin Status	0x06(Note24)	0xA2(Note25)	7(Note26)		GPIO57

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0xA1(Note28)	0(Note29)	(Note30)	GPIO50
DIO-2 Output Data	0x06(Note31)	0xA1(Note32)	1(Note33)	(Note34)	GPIO51
DIO-3 Output Data	0x06(Note35)	0xA1(Note36)	2(Note37)	(Note38)	GPIO52
DIO-4 Output Data	0x06(Note39)	0xA1(Note40)	3(Note41)	(Note42)	GPIO53
DIO-5 Output Data	0x06(Note43)	0xA1(Note44)	4(Note45)	(Note46)	GPIO54
DIO-6 Output Data	0x06(Note47)	0xA1(Note48)	5(Note49)	(Note50)	GPIO55
DIO-7 Output Data	0x06(Note51)	0xA1(Note52)	6(Note53)	(Note54)	GPIO56
DIO-8 Output Data	0x06(Note55)	0xA1(Note56)	7(Note57)	(Note58)	GPIO57

## C.4 Digital I/O Sample Program

---

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DInput1LDN // This parameter is represented from Note3
#define byte DInput1Reg // This parameter is represented from Note4
#define byte DInput1Bit // This parameter is represented from Note5
#define byte DInput2LDN // This parameter is represented from Note6
#define byte DInput2Reg // This parameter is represented from Note7
#define byte DInput2Bit // This parameter is represented from Note8
#define byte DInput3LDN // This parameter is represented from Note9
#define byte DInput3Reg // This parameter is represented from Note10
#define byte DInput3Bit // This parameter is represented from Note11
#define byte DInput4LDN // This parameter is represented from Note12
#define byte DInput4Reg // This parameter is represented from Note13
#define byte DInput4Bit // This parameter is represented from Note14
#define byte DInput5LDN // This parameter is represented from Note15
#define byte DInput5Reg // This parameter is represented from Note16
#define byte DInput5Bit // This parameter is represented from Note17
#define byte DInput6LDN // This parameter is represented from Note18
#define byte DInput6Reg // This parameter is represented from Note19
#define byte DInput6Bit // This parameter is represented from Note20
#define byte DInput7LDN // This parameter is represented from Note21
#define byte DInput7Reg // This parameter is represented from Note22
#define byte DInput7Bit // This parameter is represented from Note23
#define byte DInput8LDN // This parameter is represented from Note24
#define byte DInput8Reg // This parameter is represented from Note25
#define byte DInput8Bit // This parameter is represented from Note26
*****
```



```
*****
// Digital Output control relative definition (Please reference to Table 3)
#define byte DOutput1LDN // This parameter is represented from Note27
#define byte DOutput1Reg // This parameter is represented from Note28
#define byte DOutput1Bit // This parameter is represented from Note29
#define byte DOutput1Val // This parameter is represented from Note30
#define byte DOutput2LDN // This parameter is represented from Note31
#define byte DOutput2Reg // This parameter is represented from Note32
#define byte DOutput2Bit // This parameter is represented from Note33
#define byte DOutput2Val // This parameter is represented from Note34
#define byte DOutput3LDN // This parameter is represented from Note35
#define byte DOutput3Reg // This parameter is represented from Note36
#define byte DOutput3Bit // This parameter is represented from Note37
#define byte DOutput3Val // This parameter is represented from Note38
#define byte DOutput4LDN // This parameter is represented from Note39
#define byte DOutput4Reg // This parameter is represented from Note40
#define byte DOutput4Bit // This parameter is represented from Note41
#define byte DOutput4Val // This parameter is represented from Note42
#define byte DOutput5LDN // This parameter is represented from Note43
#define byte DOutput5Reg // This parameter is represented from Note44
#define byte DOutput5Bit // This parameter is represented from Note45
#define byte DOutput5Val // This parameter is represented from Note46
#define byte DOutput6LDN // This parameter is represented from Note47
#define byte DOutput6Reg // This parameter is represented from Note48
#define byte DOutput6Bit // This parameter is represented from Note49
#define byte DOutput6Val // This parameter is represented from Note50
#define byte DOutput7LDN // This parameter is represented from Note51
#define byte DOutput7Reg // This parameter is represented from Note52
#define byte DOutput7Bit // This parameter is represented from Note53
#define byte DOutput7Val // This parameter is represented from Note54
#define byte DOutput8LDN // This parameter is represented from Note55
#define byte DOutput8Reg // This parameter is represented from Note56
#define byte DOutput8Bit // This parameter is represented from Note57
#define byte DOutput8Val // This parameter is represented from Note58
*****
```

```
*****
VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****
```

```
*****
Boolean  AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID  AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```

```

*****
VOID  SIOEnterMBPnPMode0{
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode0{
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****

```

```
*****
Boolean  SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}
VOID  ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
    Byte TmpValue, OutputEnableReg;

    OutputEnableReg = Register-1;
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, OutputEnableReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (1 << BitNum);
    IOWriteByte(SIOData, OutputEnableReg);
    SIOExitMBPnPMode();
}
*****
```

# Appendix D

---

AI Core X

## D.1 AI Core X (PER-TAICX-A10) Manual

---

The User Manual for the AI Core X is included in this document following this section.

To view the AI Core X manual by itself, you can download a copy from the product page here:

<https://www.aaeon.com/en/p/ai-edge-computing-board-ai-core-x>

# AI Core X

---

PER-TAICX-A10-001  
Intel Myriad X mPCIe Module

User's Manual 1<sup>st</sup> Ed



## Copyright Notice

---

This document is copyrighted, 2019. All rights are reserved. The original manufacturer reserves the right to make improvements to the products described in this manual at any time without notice.

No part of this manual may be reproduced, copied, translated, or transmitted in any form or by any means without the prior written permission of the original manufacturer. Information provided in this manual is intended to be accurate and reliable. However, the original manufacturer assumes no responsibility for its use, or for any infringements upon the rights of third parties that may result from its use.

The material in this document is for product information only and is subject to change without notice. While reasonable efforts have been made in the preparation of this document to assure its accuracy, AAEMON assumes no liabilities resulting from errors or omissions in this document, or from the use of the information contained herein.

AAEMON reserves the right to make changes in the product design without notice to its users.

## Acknowledgements

---

All other products' name or trademarks are properties of their respective owners.

- Microsoft Windows® and Windows® 10 are registered trademarks of Microsoft Corp.
- Ubuntu is a registered trademark of Canonical
- Intel®, Movidius™, Myriad™, and Myriad™ X are registered trademarks of Intel Corporation
- OpenVINO™ is a registered trademark of Intel Corporation
- TensorFlow™ is a registered trademark of Google LLC
- Apache, Apache MXNet, and MXNet are registered trademarks of the Apache Software Foundation

All other product names or trademarks are properties of their respective owners. No ownership is implied or assumed for products, names or trademarks not herein listed by the publisher of this document.

## Packing List

---

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● AI Core X module card	1
● M2 screw	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

---

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the product page on [AAEON.com](http://AAEON.com) for the latest version of this document.

## Safety Precautions

---

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. Make sure the power source matches the power rating of the device.
3. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
4. Always completely disconnect the power before working on the system's hardware.
5. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
7. Always disconnect this device from any power supply before cleaning.
8. While cleaning, use a damp cloth instead of liquid or spray detergents.
9. Make sure the device is installed near a power outlet and is easily accessible.
10. Keep this device away from humidity.
11. Place the device on a solid surface during installation to prevent falls.
12. Do not cover the openings on the device to ensure optimal heat dissipation.
13. Watch out for high temperatures when the system is running.
14. Do not touch the heat sink or heat spreader when the system is running
15. Never pour any liquid into the openings. This could cause fire or electric shock.
16. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

17. If any of the following situations arises, please contact our service personnel:
  - i. Damaged power cord or plug
  - ii. Liquid intrusion to the device
  - iii. Exposure to moisture
  - iv. Device is not working as expected or in a manner as described in this manual
  - v. The device is dropped or damaged
  - vi. Any obvious signs of damage displayed on the device
18. Do not leave this device in an uncontrolled environment with temperatures beyond the device's permitted storage temperatures (see chapter 1) to prevent damage.
19. Do NOT disassemble the motherboard so as not to damage the system or void your warranty.
20. If the thermal pad had been damaged, please contact AAEON's salesperson to purchase a new one. Do NOT use those of other brands.
21. The Hex Cylinder Coppers on the front panel are not removable.
22. Repeatedly assemble and disassemble the system may cause damages to the exterior paint and surface and screw holes.
23. Use the right size screwdriver.
24. Use the screwdriver correctly to remove screws from the system.

## FCC Statement

---

### **Warning!**



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

### **Caution:**

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

### **Attention:**

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*

## China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○
<p>○: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。</p> <p>X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。</p> <p>备注: 一、此产品所标示之环保使用期限, 系指在一般正常使用状况下。 二、上述部件物质中央处理器、内存、硬盘、电源为选购品。</p>						



## China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products  
 AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○
<p>O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.</p> <p>X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.</p> <p><b>Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only</b></p>						

# Table of Contents

---

- Chapter 1 - Product Specifications ..... 1**
  - 1.1 AI Core X Specifications..... 2
- Chapter 2 – Hardware Information ..... 3**
  - 2.1 Dimensions ..... 4
  - 2.2 Block Diagram..... 5
  - 2.3 Board Design..... 6
  - 2.4 List of Connectors .....7
    - 2.4.1 mini-PCIe (CN1).....7
    - 2.4.2 Fan (CN3)..... 9
    - 2.4.3 Switch (SW1)..... 9
- Chapter 3 – Software Installation ..... 10**
  - 3.1 Intel OpenVINO Toolkit.....11

# Chapter 1

---

Product Specifications

## 1.1 AI Core X Specifications

---

### System

IC	Intel Movidius Myriad X VPU, MA2485
Supported Frameworks	Tensorflow Caffe MXNet
Supported OS	Windows 10 Ubuntu 16.04 with Intel OpenVINO

### Others

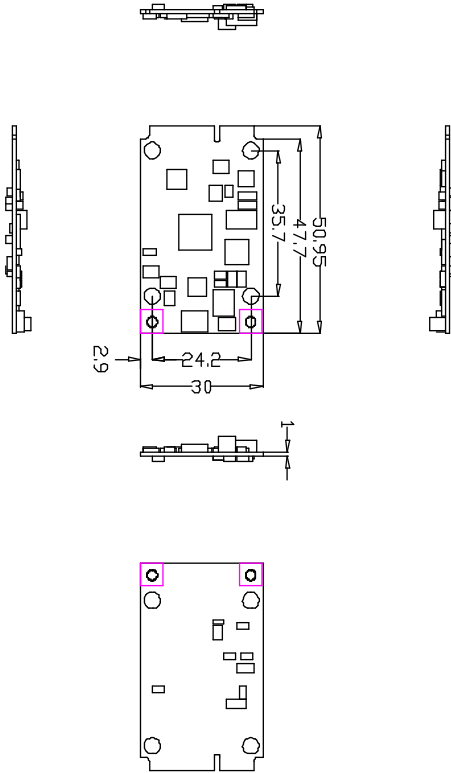
Form Factor	mini-PCIe
Dimension	51 x 30 mm
Certification	CE/FCC Class A
Operating Temperature	0~60°C
Operating Humidity	10%~80%RH, non-condensing

# Chapter 2

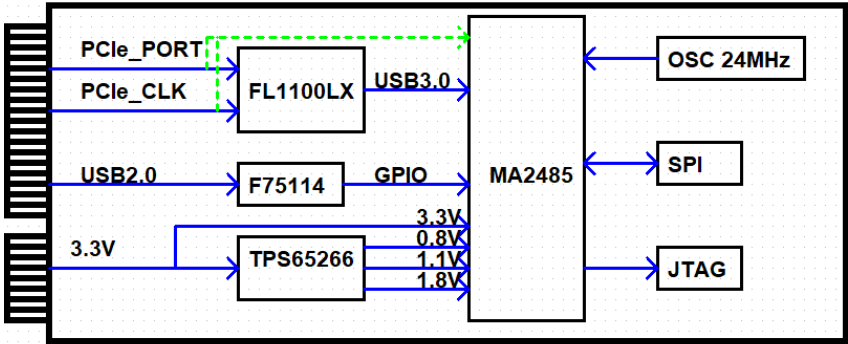
---

Hardware Information

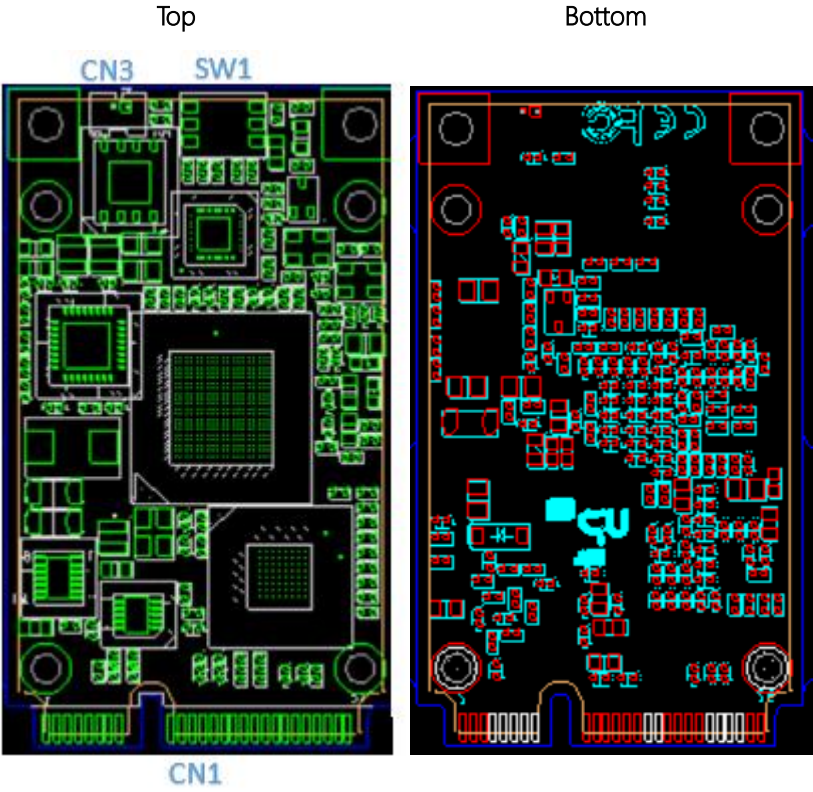
## 2.1 Dimensions



## 2.2 Block Diagram



## 2.3 Board Design





## 2.4 List of Connectors

This section details the connectors featured on the AI Core X module. This is a reference to help with setup and configuration for your application.

Label	Function	Connector Type
CN1	mini-PCIe	PCIE CONN 52pin (TF)WAFER
CN3	FAN	BOX.2P180D(M).DIP1.25mm.PINREX.712-71-02 TW01
SW1	SWITCH	(TF)SWITCH.3S.6PSOJ.24V.25mA,pitch=1.27m m.180D.SMD.BIWIN.SOJ03-R

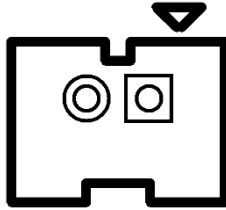
### 2.4.1 mini-PCIe (CN1)



Pin	Signal Description	Pin	Signal Description
1	WAKE#	2	3.3V
3	NC	4	GND
5	NC	6	1.5V
7	PCIE_CLKREQ#	8	NC
9	GND	10	NC
11	PCIE_CLK_N	12	NC
13	PCIE_CLK_P	14	NC
15	GND	16	NC

Pin	Signal Description	Pin	Signal Description
17	NC	18	GND
19	NC	20	DISABLE#
21	GND	22	RESET#
23	PCIE_TXN	24	3.3V
25	PCIE_TXP	26	GND
27	GND	28	1.5V
29	GND	30	NC
31	PCIE_RXN	32	NC
33	PCIE_RXP	34	GND
35	GND	36	USB2_DM
37	GND	38	USB2_DP
39	3.3V	40	GND
41	3.3V	42	NC
43	GND	44	NC
45	NC	46	NC
47	NC	48	NC
49	NC	50	GND
51	NC	52	3.3V

## 2.4.2 Fan (CN3)



Pin	Signal Description	Pin	Signal Description
1	5V	2	GND

## 2.4.3 Switch (SW1)



SW Value			Board ID
3	2	1	
Off	Off	Off	0
Off	Off	On	1
Off	On	Off	2
Off	On	On	3
On	Off	Off	4
On	Off	On	5
On	On	Off	6
On	On	On	7

# Chapter 3

---

## Software Installation

### 3.1 Intel OpenVINO Toolkit

---

The AI Core X works with Intel OpenVINO toolkit and does not require any drivers to be installed. Visit the OpenVINO website to download and install the software.

<https://software.intel.com/en-us/openvino-toolkit>