EMB-QM87A

Intel® 4th Generation Core™ i7/i5/ Celeron Processor

Mini-ITX

Gigabit Ethernet

4 USB2.0, 6 USB3.0, 6 COM

4 SATA 6.0Gb/s, 2 SATA 3.0 Gb/s

Support RAID 0,1,5,10

1 PCI-E[x16], 1 Mini-PCIe socket, 1 Optional TPM

EMB-QM87A Manual 1st Ed.
February 10th, 2014

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Acknowledgments

Packing List

(Standard, not bulk pack)

Before you begin installing your card, please make sure that the following materials have been shipped:

- 1 Jumper Cap
- 1 SATA Cable 7P
- 1 SATA PWR Cable 4P
- 1 Back I/O Shield
- 1 Product DVD-ROM
- 1 EMB-QM87A

If any of these items should be missing or damaged, please contact your distributor or sales representative immediately.

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Chapter

1

General Information

1.1 Introduction

The EMB-QM87A supports Intel® 4th Generation Intel® Core™ i7/i5/ Celeron processor which when paired with the Intel® QM87 Express chipset offers a high performance computing platform with low power consumption. This new product supports two 204-pin dual-channel DDR3L SODIMM at speeds of 1333/1600 MHz, up to 16 GB.

One Mini-PCIe socket, four SATA 6.0Gb/s and two SATA 3.0 Gb/s interfaces provide ample storages. With dual Gigabit Ethernet, six COM ports, six USB3.0, and four USB2.0, the EMB-QM87A meets the requirements of today's demanding applications.

Display requirements are met with an abundance of interfaces such as VGA, HDMI and LVDS. The graphic engine adopts 4th Generation Intel® Core™ i7 / i5 / Celeron® integrated graphics engine (Gen 8, DX11.1, OpenGL 3.2, OpenCL 1.2) to offer high definition display function.

With all of its integrated features, the EMB-QM87A strikes a balance of performance and price. This versatile product targets Industrial Automation, Entertainment, Networking, KIOSK/POS, Transportation, Banking, Healthcare and Digital Signage

applications that require high performance and high reliability.

1.2 Features

- Socket BGA 1364, Intel® 4th Generation Core™ i7/i5/Celeron Processor
- Intel® 4th Generation Core™ i7/i5/Celeron + QM87
- 204-pin Dual-channel DDR3L 1333/1600 MHz SODIMM x 2, Up to 16 GB
- Gigabit Ethernet x 2
- Dual Display Version: Dual 24-bit LVDS, VGA, HDMI
  Three Display Version: 3 x HDMI, or 2 x HDMI+VGA, or 2 x HDMI+ 24bit LVDS
- SATA 6.0Gb/s x 4, SATA 3.0Gb/s x 2, Support RAID 0,1,5,10
- USB2.0 x 4, USB3.0 x 6, COM x 6
- PCI-Express [x16] x 1, Mini-PCIe socket x 1, Optional TPM x 1

1.3 Specifications

System

From Factor	Mini-ITX
Processor	Socket BGA 1364, Intel® 4th Generation Core™ i7/i5 Processor
System Memory	204-pin Dual-channel DDR3L 1333/1600 MHz SODIMM x 2, Up to 16 GB
Chipset	Intel® Core i7/i5/Celeron + QM87
Ethernet	LAN1: Intel® Intel® Ethernet Connection I217-LM 10/100/1000Mb LANs, RJ-45 X1
	LAN2: Realtek RTL 8111E 10/100/1000Mb LANs, RJ-45 X1
BIOS	AMI BIOS 128Mbit SPI ROM
Wake On LAN	Yes
Watchdog Timer	Reset: 1 sec. ~ 255 steps programmable
H/W Status Monitoring	System temperature, voltage, and cooling fan status monitoring
Expansion Interface	PCI-E3.0 [x16] x 1
	Mini-PCIe socket x 1
	Optional TPM x 1
Battery	Lithium Battery
Power Requirement	ATX 8-pin connector for DC+12 V input x 1
	CPU fan x 1
	System fan with 4-pin wafer x 1
	SATA power with 4-pin wafer x 2

- Board Size: 6.7" x 6.7" (170mm x 170mm)
- Gross Weight: 1.32 lb (0.6Kg)
- Operating Temperature: 32°F~140°F (0°C~60°C)
- Storage Temperature: -4°F~158°F (-20°C~70°C)
- Operating Humidity: 5% ~ 90% relative humidity, non-condensing

Display: Supports CRT/LCD simultaneous / dual / triple view displays

- Chipset: Intel® Core i7/i5/Celeron + QM87
  4th Generation Intel® Core™ i7 / i5 / Celeron® integrated graphics engine
  (Gen 8, DX11.1, OpenGL 3.2, OpenCL 1.2)
- Memory: Shared system memory up to 256MB
- Resolution: Up to 4096 x 2304 @ 24Hz for 1st HDMI
  Up to 4096 x 2304 @ 24Hz for 2nd HDMI
  Up to 3840 x 2160 @ 60Hz for 3rd HDMI
  Up to 1920 x 1200 @ 60Hz for VGA
  Up to 3200 x 2000 @ 60Hz for LVDS
- Output Interface: Dual channel 24-bit LVDS, HDMI, VGA

I/O: Fintek F81866D-I

- Storage: SATA 6.0Gb/s x 4 , SATA 3.0Gb/s x 2, support RAID 0, 1, 5, 10
- Serial Port: RS-232 supports pin box header x 5 (5 x 2 box headers)
  RS-232/422/485 x 1 supports

	5/12V/RING by jumper on pin-9
● USB	USB3.0 x 6
	USB2.0 x 4
● PS/2 Port	Keyboard x 1, Mouse x 1
● Digital I/O	8-bit programmable (4-in / 4-out)
● Audio	Line-in, Mic-in, Line-out

Chapter

2

Quick Installation Guide

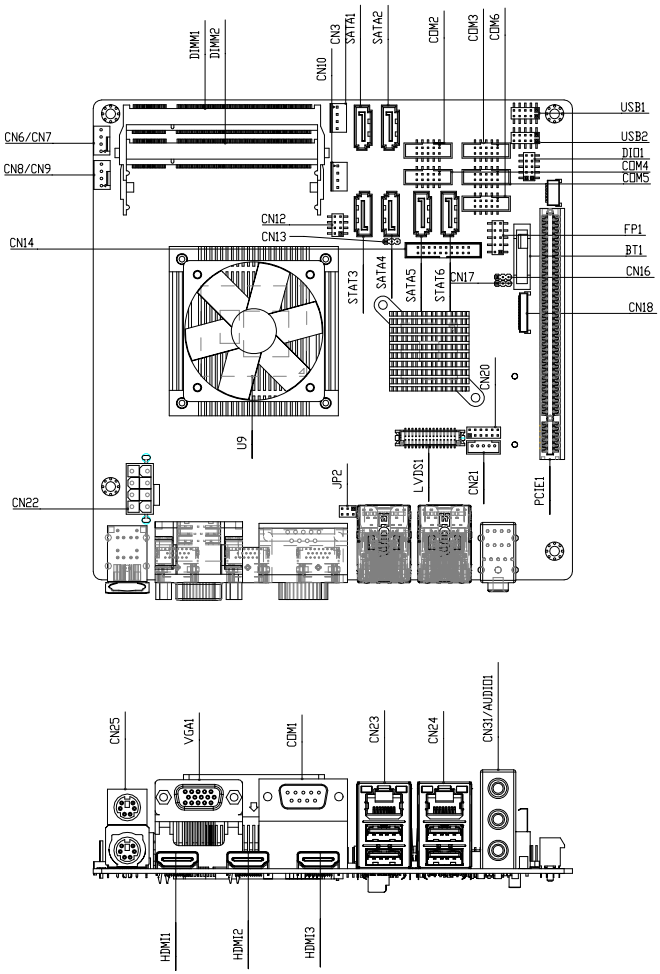
2.1 Safety Precautions

Always completely disconnect the power cord from your board whenever you are working on it. Do not make connections while the power is on, because a sudden rush of power can damage sensitive electronic components.

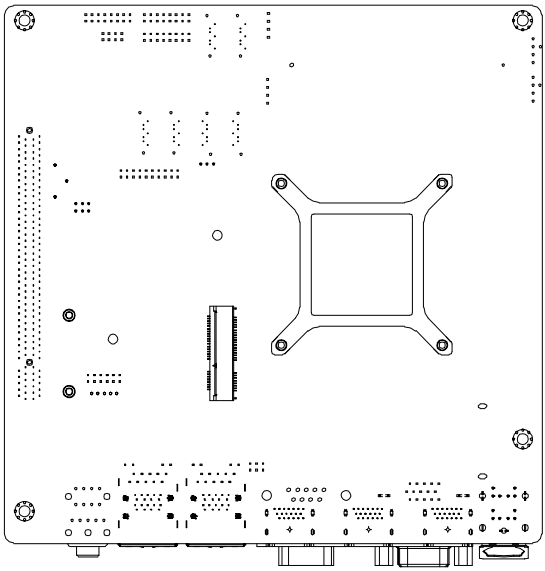
Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. Use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis

2.2 Location of Connectors and Jumpers

Component Side

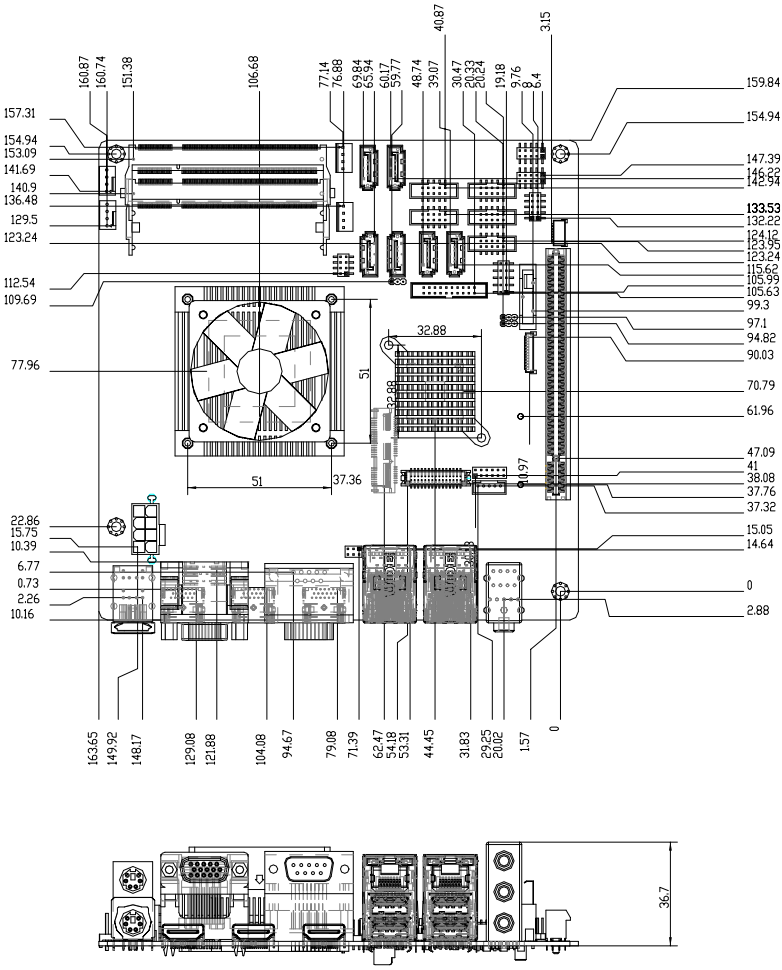


Solder Side

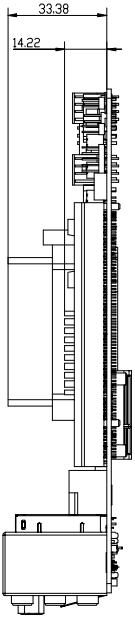


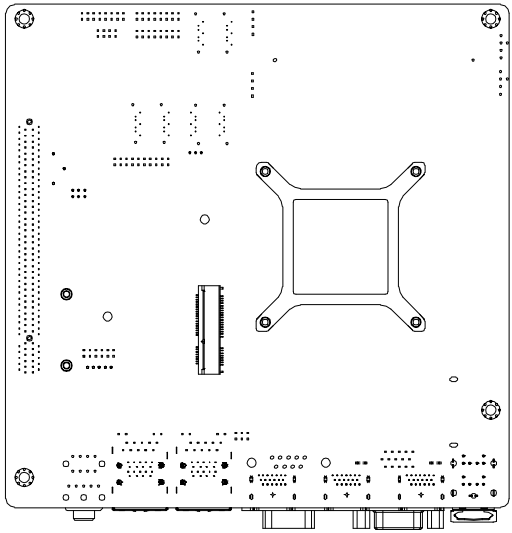
2.3 Mechanical Drawing

Component Side



Solder Side





2.4 List of Jumpers

The board has a number of jumpers that allow you to configure your system to suit your application.

The table below shows the function of each of the board's jumpers:

Label	Function
CN12	Board ID Setting
CN13	AT/ATX Select
CN16	Clear ME CMOS
CN17	Clear PCH CMOS
CN20	LVDS Setting
JP1	DDR3L Voltage Select
JP2	COM1 Ring/+5V/+12V Select

2.5 List of Connectors

The board has a number of connectors that allow you to configure your system to suit your application.

The table below shows the function of each of the board's connectors:

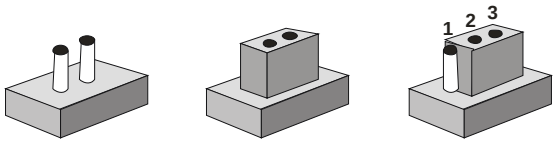
Label	Function
FP1	Front Panel Connector
VGA1	CRT_VGA Port
HDMI1~3	HDMI Port Connector
COM1	RS-232/422/485 Serial Port Connector
COM2~6	COM Port Box Header
DIO1	Digital I/O Pin Header

CN3,CN10	SATA POWER Wafer
CN6	4 Pin System Fan Connector
CN9	4 Pin CPU Fan Connector
CN11	SPI Programming Connector
CN14	USB3.0 Port BOX Header
CN18	Debug Port Connector
CN21	LVDS Inverter Power Wafer
CN22	8 pin DC-IN Power Connector
CN23,CN24	10/100/1000 Base Ethernet Connector + USB3.0 Connector
CN25	PS/2 keyboard & Mouse Connector
CN26	MINI PCIE SLOT
AUDIO1	Audio Lin-in/Lin-out/MIC
DIMM1,DIMM2	DDR3L SODIMM Slot
USB1,USB2	USB2.0 Port Pin Header
SATA1,2,5,6	SATA 3 Connector
SATA 3,4	SATA 2 Connector
PCIE1	PCI-Ex16 Slot
LVDS1	LVDS Connector

2.6 Setting Jumpers

You configure your card to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip.

To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



Open **Closed** **Closed 2-3**

A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any change.

Generally, you simply need a standard cable to make most connections.

2.7 AT/ATX Select (CN13)

CN13	Function
1-2	ATX (Default)
2-3	AT

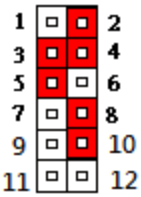
2.8 Clear ME (CN16)

CN16	Function
1-2	Normal (Default)
2-3	Clear CMOS

2.9 Clear PCH CMOS (CN17)

CN17	Function
1-2	Normal (Default)
2-3	Clear CMOS

2.10 LVDS Setting & Inverter Voltage Selection (CN20)



LVDS Panel Voltage Select

CN20	Function
1-3	+5V
3-5	+3.3V (Default)

LVDS Inverter Voltage Select

CN20	Function

2-4	+5V (Default)
4-6	+12V

LVDS Backlight Brightness Control

CN20	Function
8-10	Voltage Mode (Default)
10-12	PWM Mode

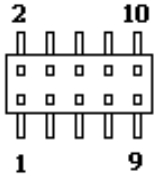
2.11 DDR3L Voltage Select (JP1)

CN13	Function
1-2	1.35V (Default)
OFF	1.5V

2.12 COM1 Ring/+5V/+12V Select (JP2)

JP5	Function
1-2	+12V
3-4	Ring (Default)
5-6	+5V

2.13 Front Panel Pin Header (FP1)

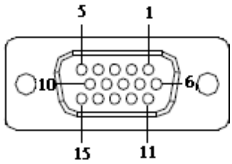


Pin	Signal	Pin	Signal
1	Power On Button (-)	2	Power On Button (+)
3	HDD LED (-)	4	HDD LED (+)

5	SPEAKER(-)	6	SPEAKER(+)
7	Power LED (-)	8	Power LED (+)
9	Reset Switch (-)	10	Reset Switch (+)

Note: The max. rating of pin1,2,3,4,7,8 is 0.25A @ 5V

2.14 VGA Port Connector (VGA1)



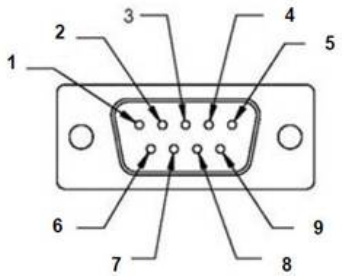
Pin	Signal	Pin	Signal
1	Red	2	Green
3	Blue	4	N.C.
5	GND	6	GND
7	GND	8	GND
9	+5V_CRT	10	GND
11	CRT_PLUG#	12	DDC_DATA
13	CRT_OHSYNCF	14	CRT_OVSYNCF
15	DDC_CLK		

Note: The max. rating of pin9 is 1.5A @ 5V

2.15 HDMI Port Connector (HDMI1~3)

Pin	Signal	Pin	Signal
1	DATA2_P	2	GND
3	DATA2_N	4	N.C.
5	GND	6	DATA1_P
7	DATA0_P	8	DATA1_N
9	DATA0_N	10	GND
11	GND	12	CLK_P
13	N.C.	14	CLK_N
15	DDC_CLK	16	N.C.
17	GND	18	DDC_DATA
19	HPD	20	

2.16 COM Port Connector (COM1)



RS-232

Pin	Signal	Pin	Signal
1	DCD1	2	RXD1
3	TXD1	4	DTR1
5	GND	6	DSR1

7	RTS1	8	CTS1
9	RI1/5V/12V	10	

RS-422

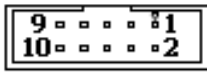
Pin	Signal	Pin	Signal
1	RS422_TX-	2	RS422_RX+
3	RS422_TX+	4	RS422_RX-
5	GND	6	NC
7	NC	8	NC
9	NC/5V/12V	10	

RS-485

Pin	Signal	Pin	Signal
1	RS485_D-	2	NC
3	RS485_D+	4	NC-
5	GND	6	NC
7	NC	8	NC
9	NC/5V/12V	10	

Note: The max. rating of pin9 is 1A @ 5V & 12V

2.17 COM Port Box Header (COM2~6)

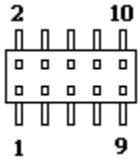


Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR

5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	NC

Note: The max. rating of pin9 is 1A @ 5V & 12V

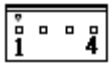
2.18 Digital I/O Pin Header (DIO1)



Pin	Signal	Pin	Signal
1	IN0	2	IN1
3	IN2	4	IN3
5	OUT0	6	OUT1
7	OUT2	8	OUT3
9	+3.3V	10	GND

Note: The max. rating of pin9 is 0.5A @ 3.3V

2.27 SATA Power Wafer (CN3,CN10)

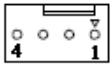


Pin	Signal	Pin	Signal
1	+12V	2	GND
3	GND	4	+5V

Note: The max. rating of pin1 is 1 A @ 12V

The max. rating of pin5 is 1 A @ 5V

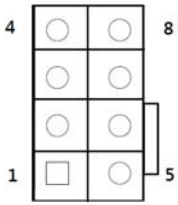
2.22 4 PIN Fan Wafer (CN9,CN6)



Pin	Signal	Pin	Signal
1	GND	2	+12V
3	FAN_TAC	4	FAN_CTL

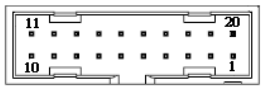
Note: The max. rating of pin2 is 1A @ 12V

2.23 8 pin DC-IN Power Connector Power (CN22)



Pin	Signal	Pin	Signal
1	GND	2	GND
3	GND	4	GND
5	+12V	6	+12V
7	+12V	8	+12V

2.21 USB3.0 Box Header (CN23)

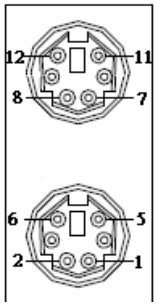


Pin	Signal	Pin	Signal
1	+5V_USB	2	P1_SSRX-
3	P1_SSRX+	4	GND
5	P1_SSTX-	6	P1_SSTX+
7	GND	8	P1_D-
9	P1_D+	10	N.C.
11	P2_D+	12	P2_D-
13	GND	14	P2_SSTX+
15	P2_SSTX-	16	GND
17	P2_SSRX+	18	P2_SSRX-
19	+5V_USB	20	N.C.

Note: The max. rating of pin1 is 0.9A @ 5V

The max. rating of pin19 is 0.9A @ 5V

2.19 PS/2 keyboard & Mouse Connector (CN25)



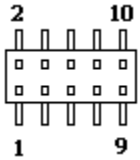
Pin	Signal	Pin	Signal
1	KB_DATA	2	N.C.

3	GND	4	+5V_KB
5	KB_CLK	6	N.C.
7	MS_DATA	8	N.C.
9	GND	10	+5V_KB
11	MS_CLK	12	N.C.

Note: The max. rating of pin4 is 0.275A @ 5V

The max. rating of pin10 is 0.275A @ 5V

2.20 USB Connector (USB1,USB2)

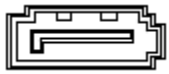


Pin	Signal	Pin	Signal
1	+5V_USB	2	GND
3	USB1_N	4	GND
5	USB1_P	6	USB2_P
7	GND	8	USB2_N
9	GND	10	+5V_USB

Note: The max. rating of pin 1 is 0.5A @ 5V

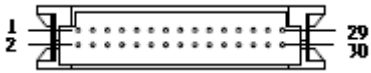
The max. rating of pin 10 is 0.5A @ 5V

2.24 SATA Port Connector (SATA1~6)



Pin	Signal	Pin	Signal
1	GND	2	SATA_TXP
3	SATA_TXN	4	GND
5	SATA_RXN	6	SATA_RXP
7	GND		

2.25 LVDS Connector (LVDS1)

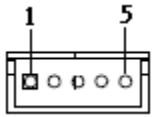


Pin	Signal	Pin	Signal
1	BKLT_EN	2	BKLT_CTRL
3	LVDSVCC	4	GND
5	LVDS1_CLK#	6	LVDS1_CLK
7	LVDSVCC	8	GND
9	LVDS1_DATA0#	10	LVDS1_DATA0
11	LVDS1_DATA1#	12	LVDS1_DATA1
13	LVDS1_DATA2#	14	LVDS1_DATA2
15	LVDS1_DATA3#	16	LVDS1_DATA3
17	LVDS_DDC_DATA	18	LVDS_DDC_CLK
19	LVDS2_DATA0#	20	LVDS2_DATA0
21	LVDS2_DATA1#	22	LVDS2_DATA1
23	LVDS2_DATA2#	24	LVDS2_DATA2

25	LVDS2_DATA3#	26	LVDS2_DATA3
27	LVDSVCC	28	GND
29	LVDS2_CLK#	30	LVDS2_CLK

Note: The max. rating of pin3,7 is 2A @ 5V / 3.3V

2.26 LVDS Inverter Power Wafer (CN21)



Pin	Signal	Pin	Signal
1	12V / 5V	2	VCON
3	GND	4	GND
5	INV_EN		

Note: The max. rating of pin1 is 2A @ 12V / 5V

Below Table for China RoHS Requirements
产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板及其电子组件	×	O	O	O	O	O
外部信号连接器及线材	×	O	O	O	O	O

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 **SJ/T 11363-2006** 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 **SJ/T 11363-2006** 标准规定的限量要求。

备注：此产品所标示之环保使用期限，系指在一般正常使用状况下。

Chapter

3

AMI BIOS Setup

3.1 System Test and Initialization

These routines test and initialize board hardware. If the routines encounter an error during the tests, you will either hear a few short beeps or see an error message on the screen. There are two kinds of errors: fatal and non-fatal. The system can usually continue the boot up sequence with non-fatal errors.

System configuration verification

These routines check the current system configuration stored in the CMOS memory and BIOS NVRAM. If system configuration is not found or system configuration data error is detected, system will load optimized default and re-boot with this default system configuration automatically.

There are four situations in which you will need to setup system configuration:

1. You are starting your system for the first time
2. You have changed the hardware attached to your system
3. The system configuration is reset by Clear-CMOS jumper
4. The CMOS memory has lost power and the configuration information has been erased.

The EMB-QM87A CMOS memory has an integral lithium battery backup for data retention. You will need to replace the battery when

it finally runs down.

3.2 AMI BIOS Setup

AMI BIOS ROM has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in battery-backed CMOS RAM and BIOS NVRAM so that it retains the Setup information when the power is turned off.

Entering Setup

Power on the computer and press <Del>or <F2> immediately. This will allow you to enter Setup.

Main

Set the date, use tab to switch between date elements.

Advanced

Enable disable boot option for legacy network devices.

Chipset

Host bridge parameters.

Boot

Enables/disable quiet boot option.

Security

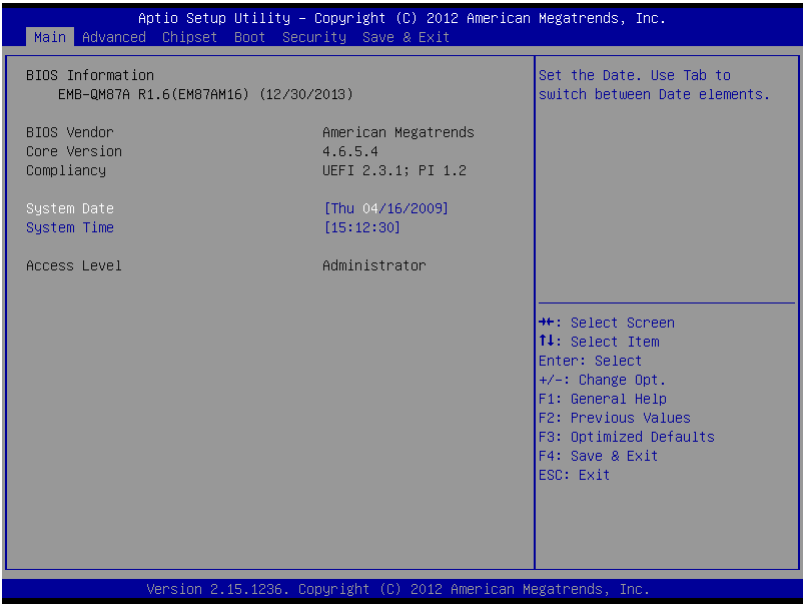
Set setup administrator password.

Save&Exit

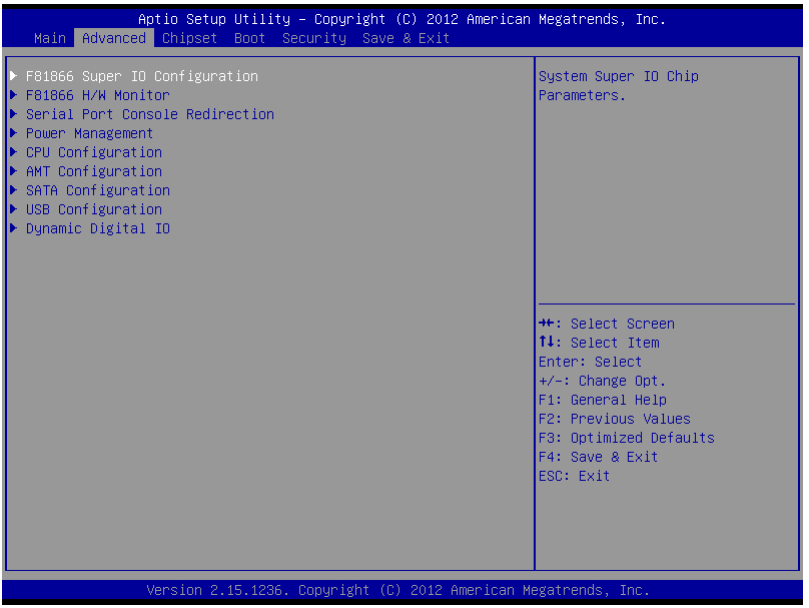
Exit system setup after saving the changes.

Setup Menu

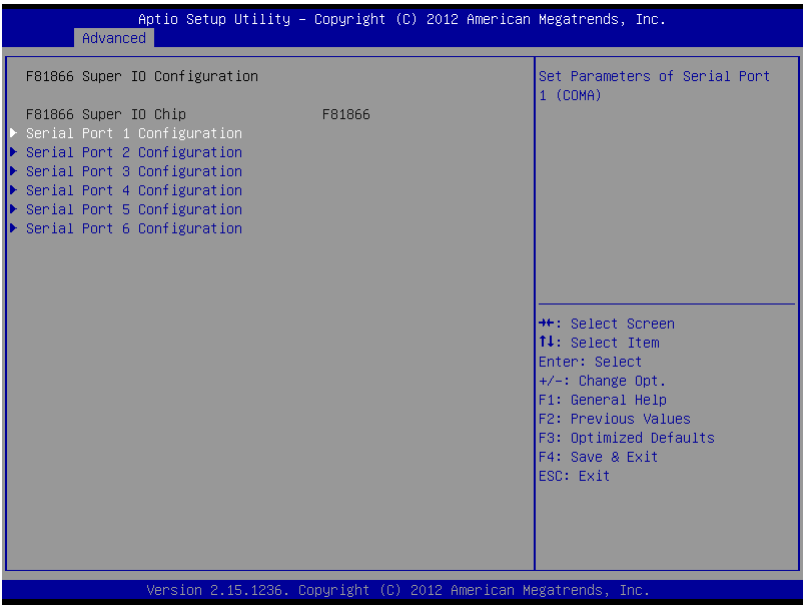
Setup submenu: Main



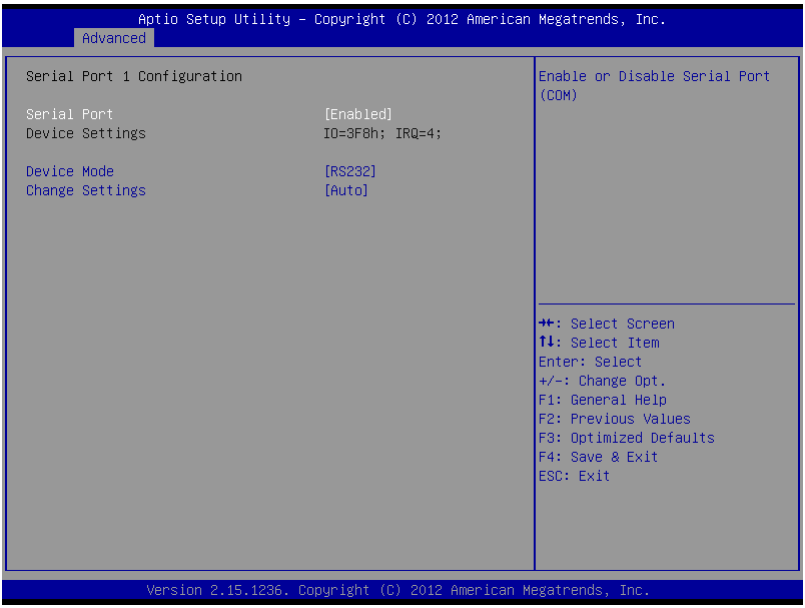
Setup submenu: Advanced



Super IO Configuration



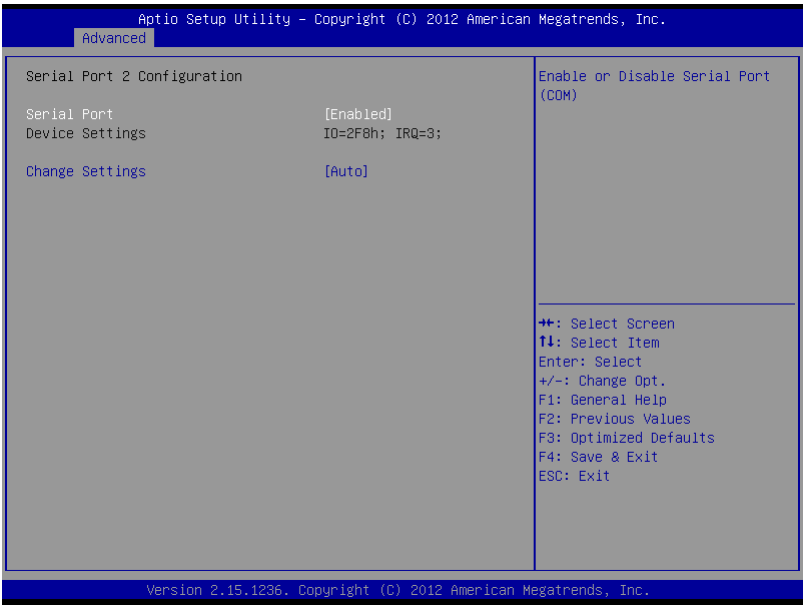
Serial Port 1 Configuration



Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Device Mode	**RS232**
	RS422
	RS485
Select working model	
Serial Port	**Auto**
	IO=3F8h; IRQ=4;
	IO=3F8h; IRQ=3,4
	IO=2F8h; IRQ=3,4
	IO=3E8h; IRQ=3,4
	IO=2E8h; IRQ=3,4
Select an optimal setting for Super IO device.	

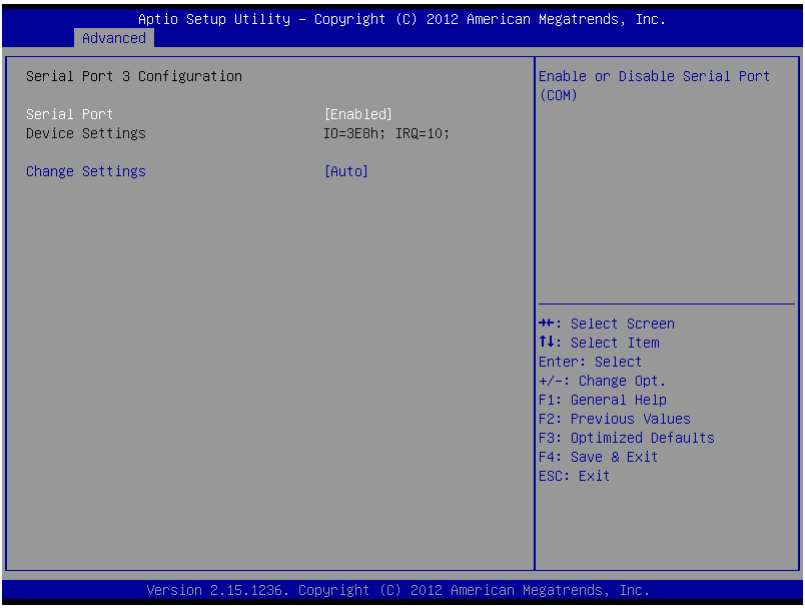
Serial Port 2 Configuration



Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Serial Port	**Auto**
	IO=2F8h; IRQ=3;
	IO=3F8h; IRQ=3,4
	IO=2F8h; IRQ=3,4
	IO=3E8h; IRQ=3,4
	IO=2E8h; IRQ=3,4
Select an optimal setting for Super IO device.	

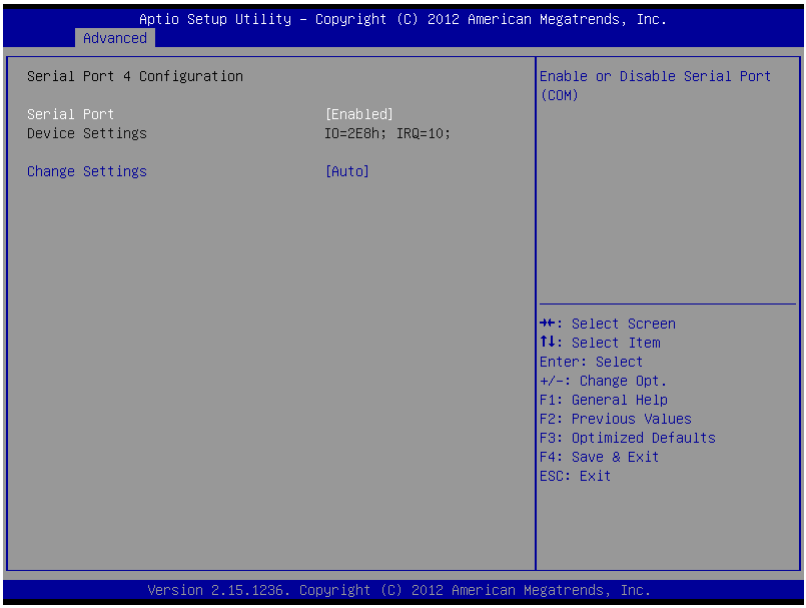
Serial Port 3 Configuration



Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Serial Port	**Auto**
	IO=3E8h; IRQ=10,
	IO=3E8h; IRQ=10,
	IO=2E8h; IRQ=10,
	IO=2D0h; IRQ=10,
	IO=2C0h; IRQ=10,
Select an optimal setting for Super IO device.	

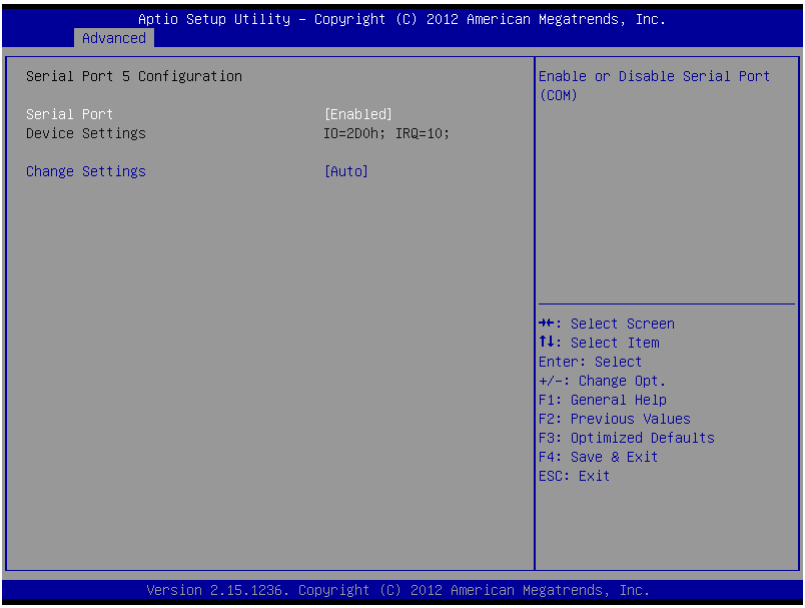
Serial Port 4 Configuration



Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Serial Port	**Auto**
	IO=2E8h; IRQ=10,
	IO=3E8h; IRQ=10,
	IO=2E8h; IRQ=10,
	IO=2D0h; IRQ=10,
	IO=2C0h; IRQ=10,
Select an optimal setting for Super IO device.	

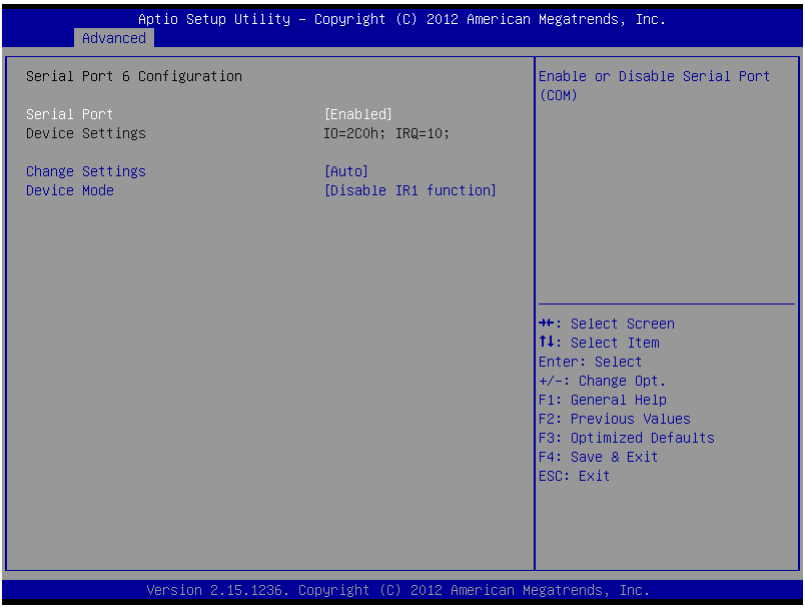
Serial Port 5 Configuration



Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Serial Port	**Auto**
	IO=2D0h; IRQ=10,
	IO=3E8h; IRQ=10,
	IO=2E8h; IRQ=10,
	IO=2D0h; IRQ=10,
	IO=2C0h; IRQ=10,
Select an optimal setting for Super IO device.	

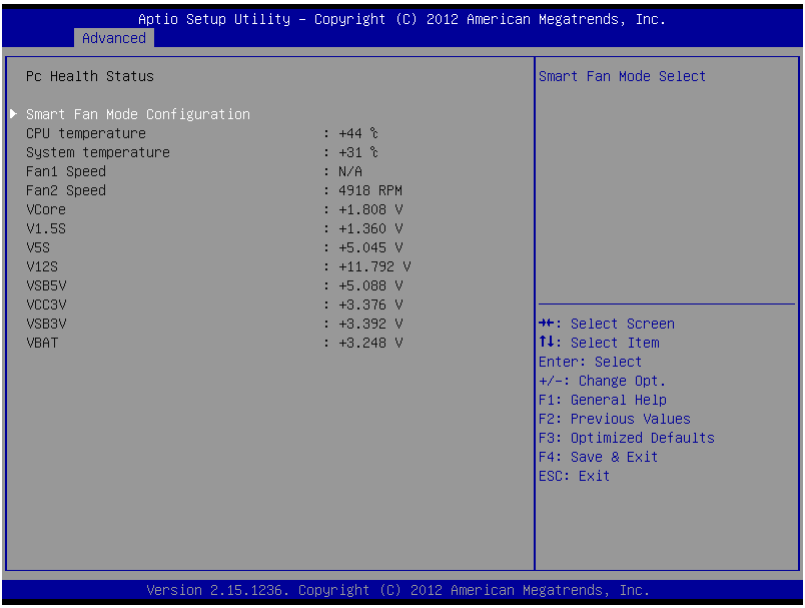
Serial Port 6 Configuration



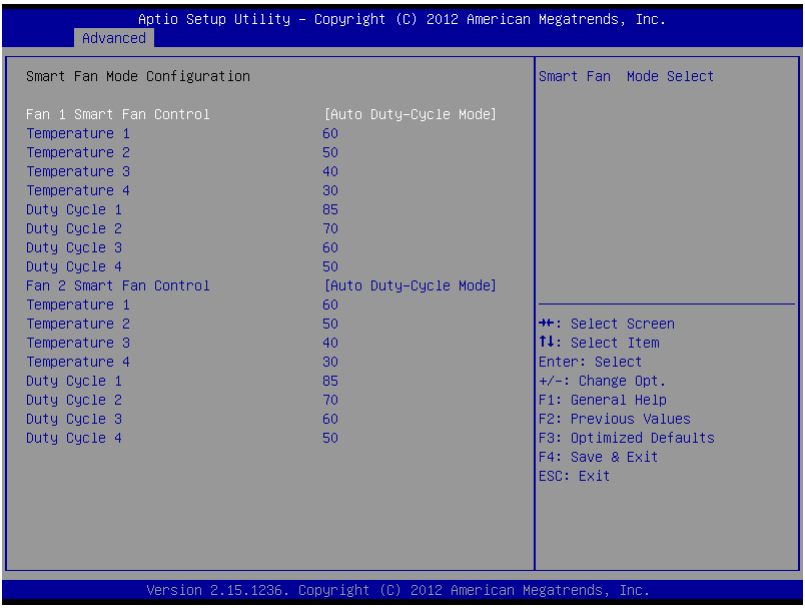
Options summary:

Serial Port	Disabled
	Enabled
Enable or Disable Serial Port (COM)	
Serial Port	**Auto**
	IO=2C0h; IRQ=10,
	IO=3E8h; IRQ=10,
	IO=2E8h; IRQ=10,
	IO=2D0h; IRQ=10,
	IO=2C0h; IRQ=10,
Select an optimal setting for Super IO device.	

H/W Monitor


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
Pc Health Status
Smart Fan Mode Configuration
CPU temperature : +44 °C
System temperature : +31 °C
Fan1 Speed : N/A
Fan2 Speed : 4918 RPM
VCore : +1.808 V
V1.5S : +1.360 V
V5S : +5.045 V
V12S : +11.792 V
VSB5V : +5.088 V
VCC3V : +3.376 V
VSB3V : +3.392 V
VBAT : +3.248 V
Smart Fan Mode Select
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1236. Copyright (C) 2012 American Megatrends, Inc.

Smart Fan Function

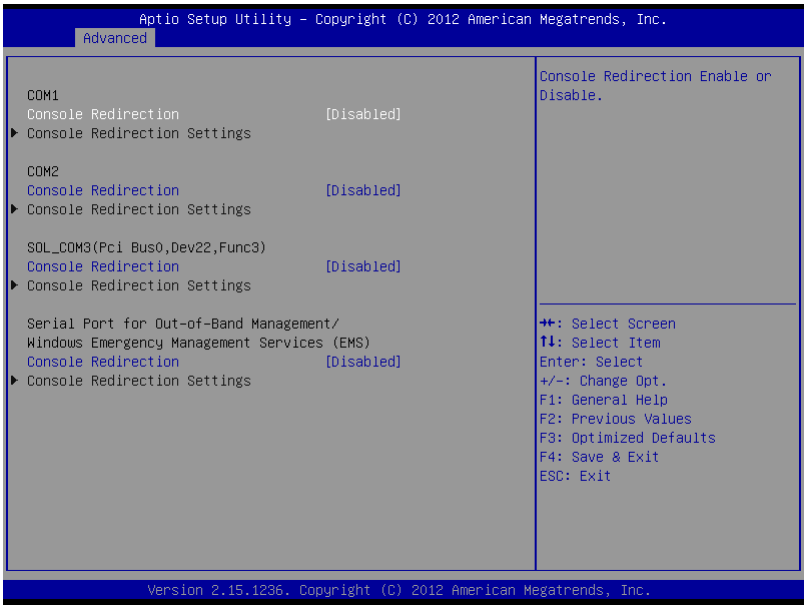


Options summary:

Fan 1,2 Smart Fan Mode	Manual RPM Mode
	Manual Duty Mode
	Auto RPM Mode
	Auto Duty-Cycle Mode
Smart Fan Mode Select	
Fan off temperature limit	**15 (0-127)**
Fan will of when temperature lower than this limit.	
Fan start temperature limit	**45 (0-127)**
Fan will work when temperature higher than this limit.	
Fan start PWM	**35 (0-255)**
Fan will start with this PWM value(Range 0-255).	

PWM SLOPE SETTING	0.125 PWM
	0.25 PWM
	0.5 PWM
	1 PWM
	2 PWM
	4 PWM
	8 PWM
	15.875 PWM
PWM SLOPE Selection	

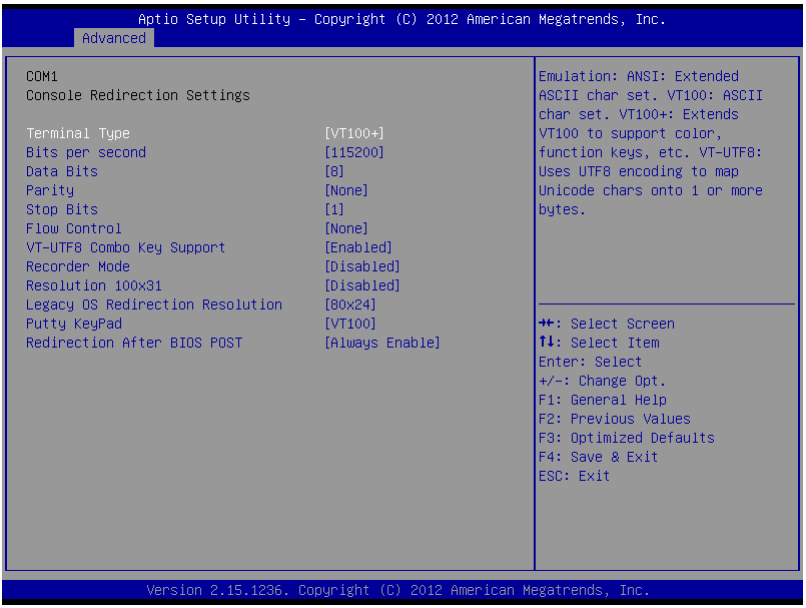
Serial Port Cons



Options summary:

Console Redirection	**Disabled**
	Enabled
Console Redirection Enabled or Disabled.	

Console Redirection Settings



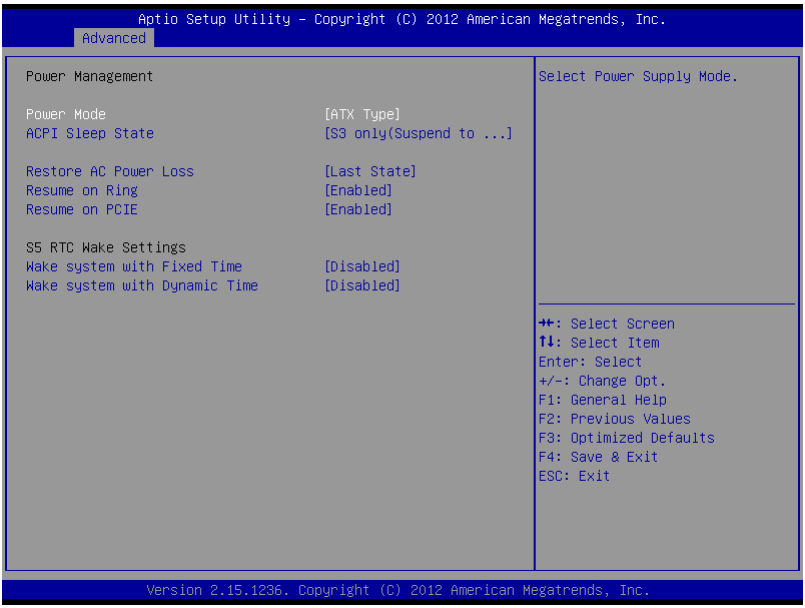
Options summary:

Terminal Type	VT100
	VT100+
	VT-UTF8
	ANSI
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.	
Bits per second	9600
	19200
	38400
	57600
	115200
Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.	
Data Bits	7
	8
Data Bits	

Parity	**None**
	Even
	Odd
	Mark
	Space
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0. Mark and Space Parity do not allow for error detection.	
Stop Bits	**1**
	2
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.	
Flow Control	**None**
	Hardware RTS/CTS
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	

VT-UTF8 Combo Key Support	Disabled
	Enabled
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals	
Recorder Mode	**Disabled**
	Enabled
On this mode enabled only text will be send. This is to capture Terminal data.	
Resolution 100x31	Disabled
	Enabled
Enables or disables extended terminal resolution	
Legacy OS Redirection Resolution	**80x24**
	80x25
On Legacy OS, the Number of Rows and Columns supported redirection	
Putty KeyPad	**VT100**
	LINUX
	XTERMR6
	SCO
	ESCN
	VT400
Select FunctionKey and KeyPad on Putty.	
Redirection After BIOS POST	**Always Enable**
	BootLoader
The Setting Specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is Always Enable which means Legacy console Redirection is enabled for Legacy OS.	

Power Management

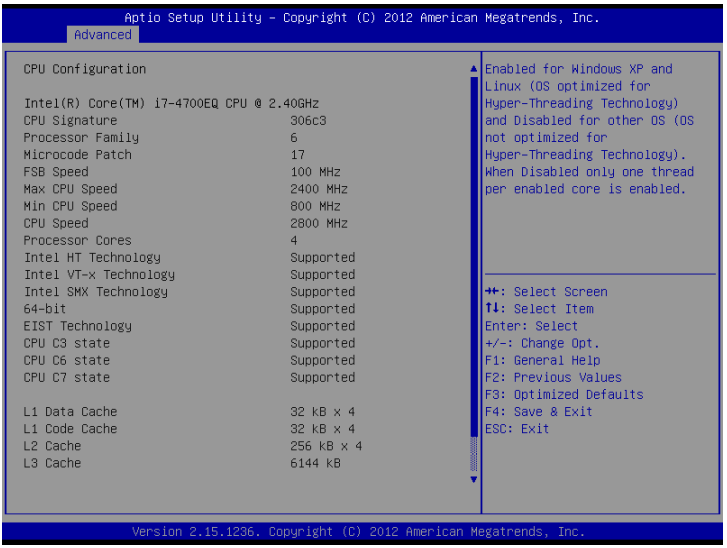


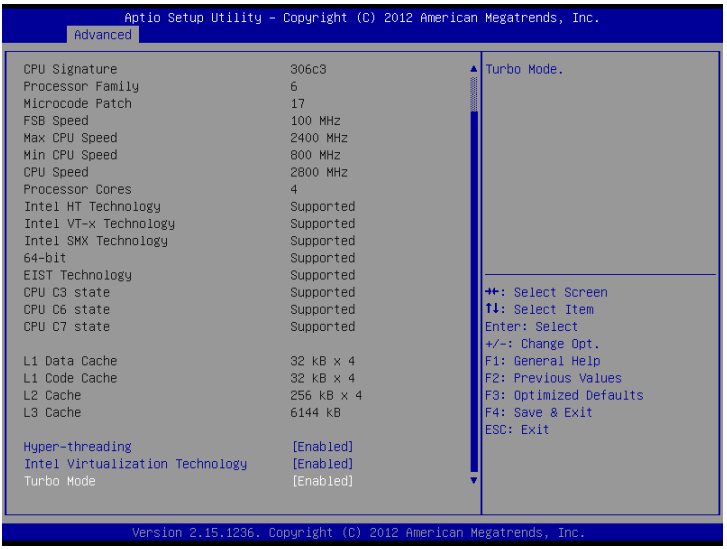
Options summary:

Power Mode	**ATX Type**
	AT Type
Select Power Supply Mode.	
ACPI Sleep State	Suspend Disabled
	S3 only (Suspend to RAM)
Select ACPI sleep state the system will enter when the SUSPEND button is pressed.	
Restore AC Power Loss	Power Off
	Power On
	Last State
Select AC power state when power is re-applied after a power failure.	
Resume on Ring	Disabled
	Enabled
Enable/Disable Resume from RI# signal.	
Resume on PCIE	Disabled
	Enabled
Enable/Disable Resume from PCIE signal.	
Wake system with Fixed Time	**Disabled**

	Enabled
Enable or disable System wake on alarm event. When enable, System will wake on the hr::min::sec specified.	
Wake up day	**0**
Select 0 for daily system wake up, 1-31 for which day of month that you would like the system to wake up.	
Wake up hour	**0**
Select 0-23 For example enter 3 for 3am and 15 for 3pm.	
Wake up minute	**0**
0-59	
Wake up second	**0**
0-59	
Wake system with Dynamic Time	Disabled
	Enabled
Enable or disable System wake on alarm event. When enabled, System will wake on the current time + Increase minute(s).	
Wake up minute increase	1
1-5	

CPU Configuration

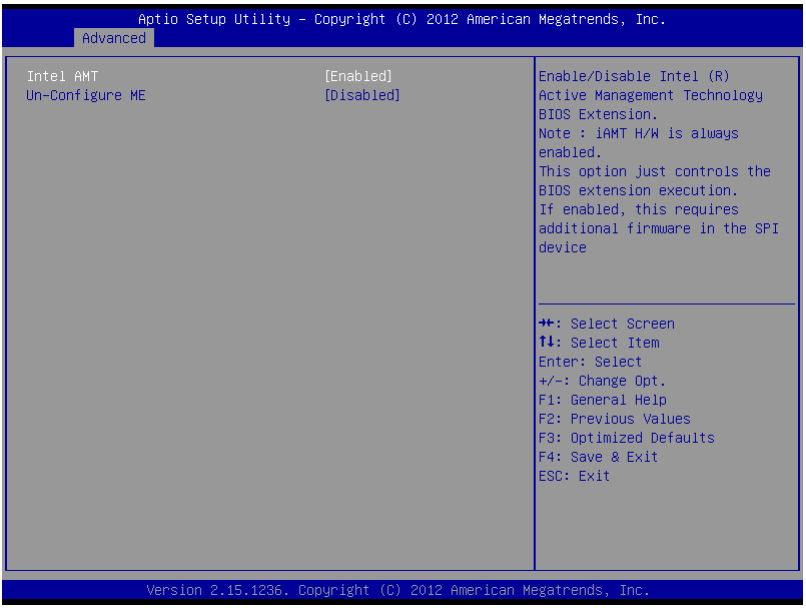




Options summary :

Hyper-threading	Disabled
	Enabled
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled only on thread per enabled core is enabled.	
Intel Virtualization Technology	Disabled
	Enabled
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.	
Turbo Mode	Disabled
	Enabled
Turbo Mode	

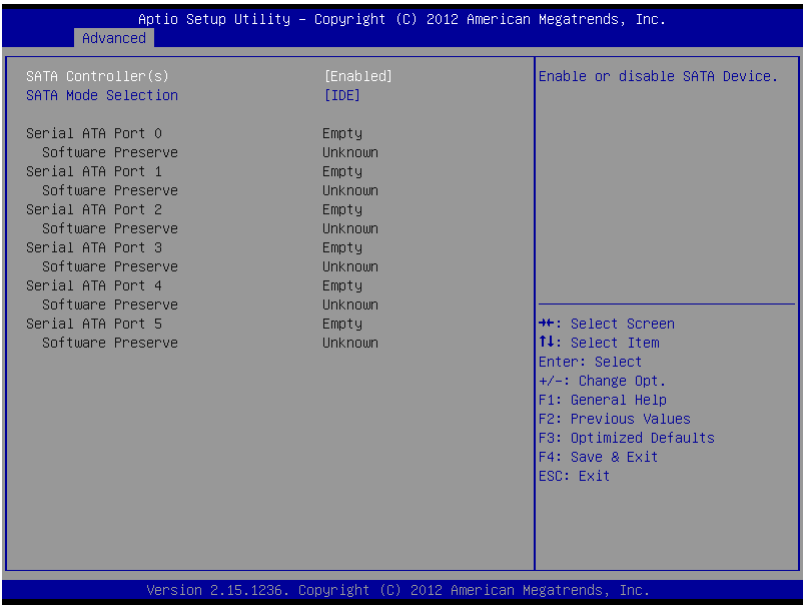
AMT Configuration



Options summary:

Intel AMT	Disabled
	Enabled
Enable/Disable Intel ® Active Management Technology BIOS Extension. Note : iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device	
Un-Configure ME	Disabled
	Enabled
OEMFlag Bit 15: Un-Configure ME without password.	

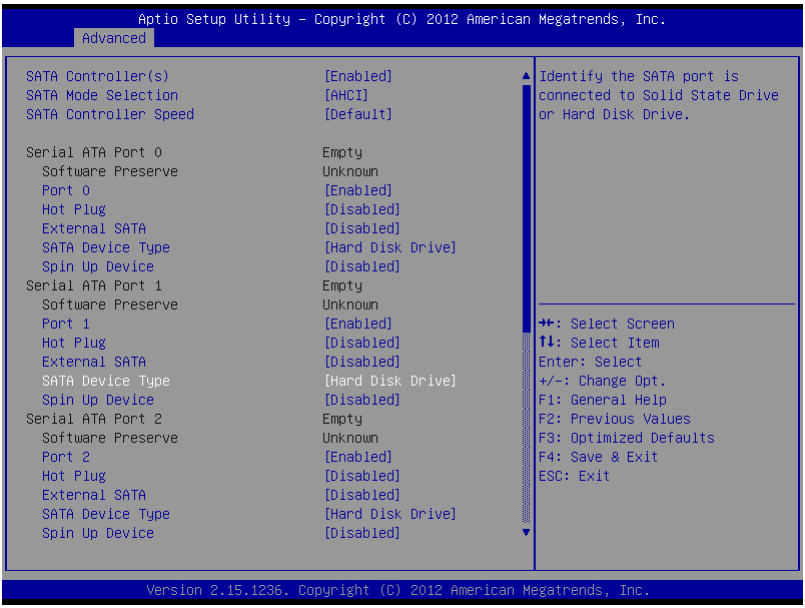
SATA Configuration (IDE)



Options summary :

SATA Controller(s)	Disabled
	Enabled
Enable or disable SATA Device.	
SATA Mode Selection	**IDE**
	AHCI
	RAID
Determines how SATA controller(s) operate.	

SATA Configuration (AHCI)

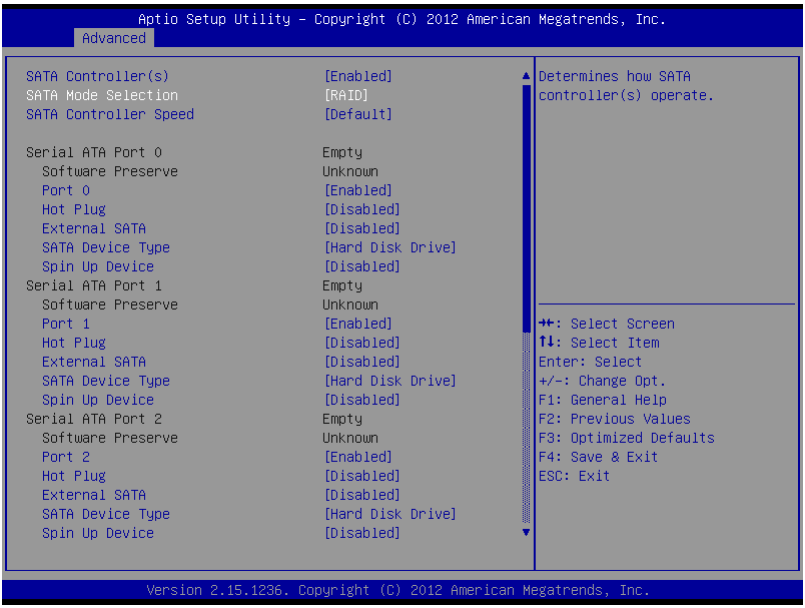


Options summary :

SATA Controller Speed	Disabled
	Enabled
Enable or disable SATA Device.	
SATA Mode Selection	**Default**
	Gen1
	Gen2
	Gen3
Indicates the maximum speed the SATA controller can support.	
Port	Disabled
	Enabled
Enable or Disable SATA Port	
Hot Plug	Disabled
	Enabled
Designates this port as Hot Pluggable.	
External SATA	Disabled
	Enabled
External SATA Support.	

SATA Device Type	**Hard Disk Drive**
	Solid State Drive
Indentify the SATA port is connected to Solid State Drive or Hard Disk Drive.	
Spin Up Device	**Disabled**
	Enabled
On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to device.	

SATA Configuration (RAID)

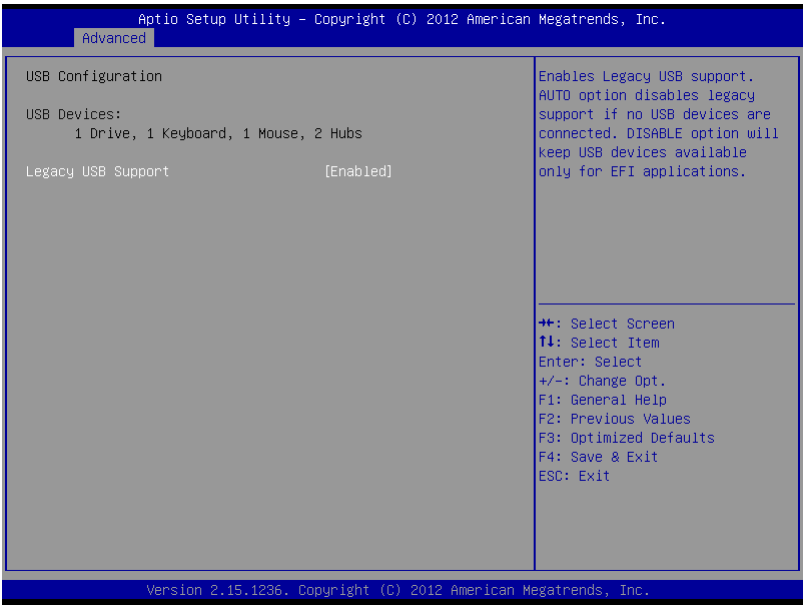


Options summary :

SATA Controller Speed	Disabled
	Enabled
Enable or disable SATA Device.	
SATA Mode Selection	**Default**
	Gen1
	Gen2
	Gen3
Indicates the maximum speed the SATA controller can support.	
Port	Disabled
	Enabled
Enable or Disable SATA Port	
Hot Plug	Disabled
	Enabled
Designates this port as Hot Pluggable.	
External SATA	Disabled
	Enabled
External SATA Support.	

SATA Device Type	**Hard Disk Drive**
	Solid State Drive
Indentify the SATA port is connected to Solid State Drive or Hard Disk Drive.	
Spin Up Device	**Disabled**
	Enabled
On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to device.	

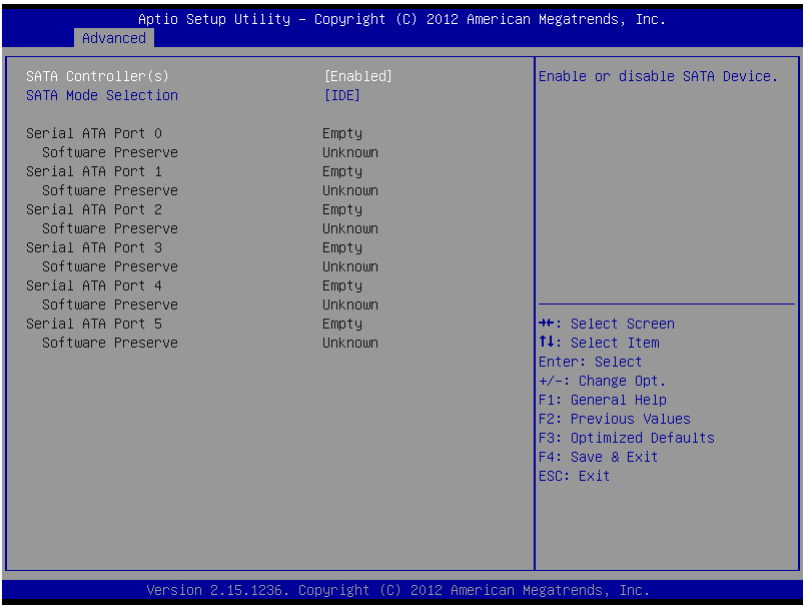
USB Configuration



Options summary:

Legacy USB Support	**Enabled**
	Disabled
	Auto
Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB device available only for EFI applications.	

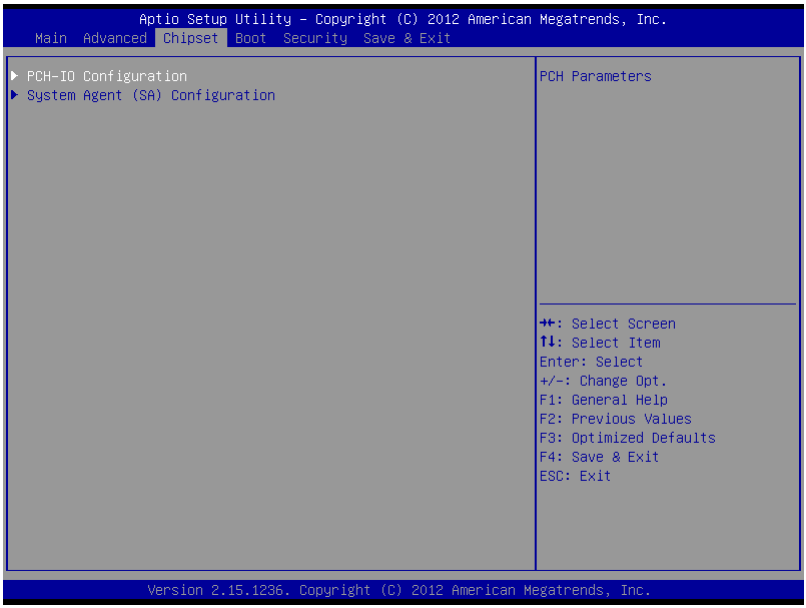
Dynamic Digital IO



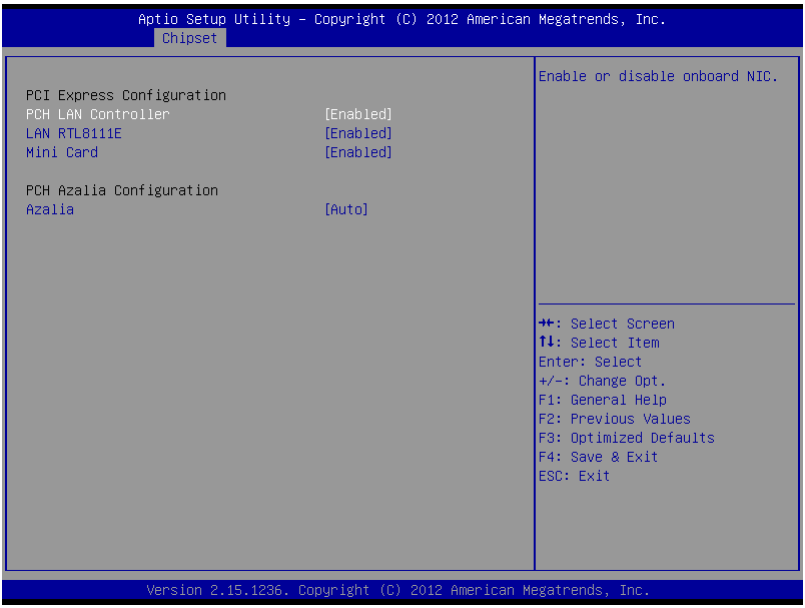
Options Summary:

DIOx Direction	Input **(DIO0,1,2,3)**
	Output **(DIO4,5,6,7)**
Set Digital IO as Input or Output	
Output Level	**Hi**
	Low
Set Digital IO Output as Hi or Low	

Setup submenu: Chipset



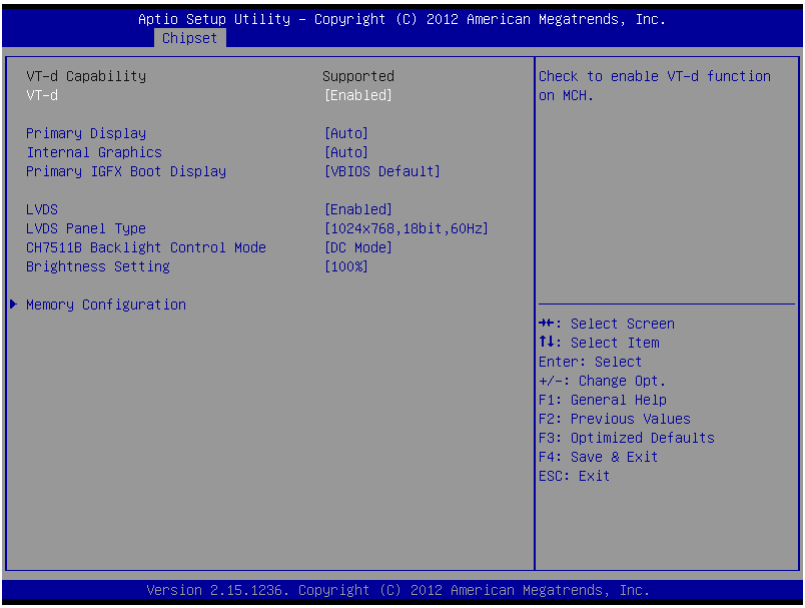
PCH-IO Configuration



Options summary:

PCH LAN Controller	**Enabled**
	Disabled
Enable or disable onboard NIC.	
LAN RTL8111E	Disabled
	Enabled
Control the PCI Express Root Port.	
Mini Card	Disabled
	Enabled
Control the PCI Express Root Port.	
Aazlia	Disabled
	Enabled
	Auto
Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled Enabled = Azalia will be unconditionally Enabled Auto = Azalia will be enabled If present , disabled otherwise.	

System Agent (SA) Configuration

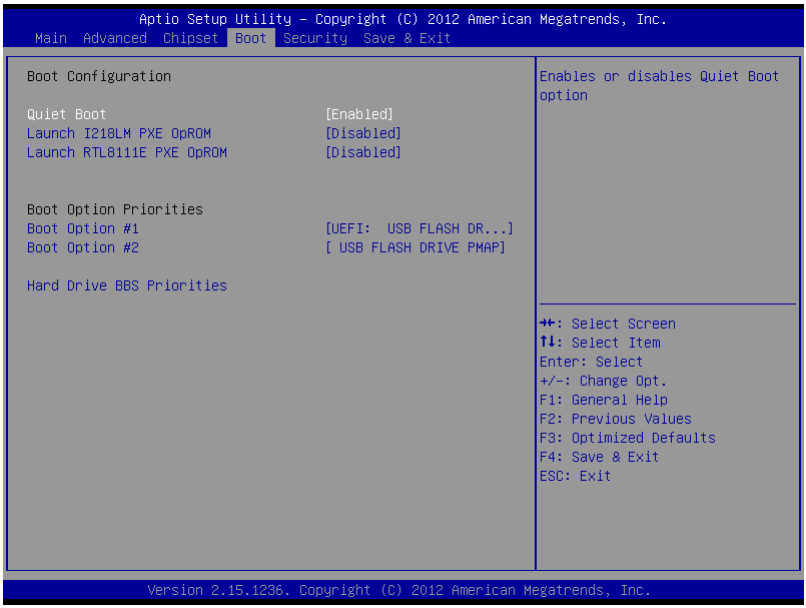


Options summary :

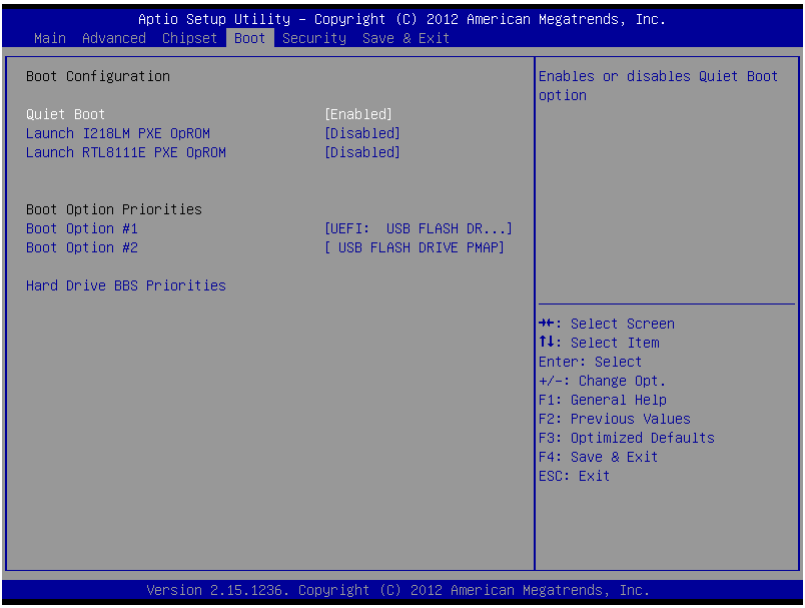
VT-d	Disabled
	Enabled
Check to enable VT-d function on MCH.	
Primary Display	**Auto**
	IGFX
	PEG
	PCIE
Select which of IGFX/PEG/PCI Graphic device should be Primary Display.	
Internal Graphics	Auto
	Disabled
	Enabled
Keep IGD enabled base on the setup options.	
Primary IGFX Boot Display	**VBIOS Default**
	CRT
	LVDS
	HDMI1
	HDMI2
	HDMI3

Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.	
Secondary IGFX Boot Display	**Disabled**
	CRT
	LVDS
	HDMI1
	HDMI2
	HDMI3
Select Secondary Display Device.	
LVDS	Disabled
	Enabled
LVDS(CH7511) Enabled/Disabled	
LVDS Panel Type	640x480,18bit,60Hz
	800x480,18bit,60Hz
	800x600,18bit,60Hz
	1024x600,18bit,60Hz
	1024x768,18bit,60Hz
	1024x768,24bit,60Hz
	1280x768,24bit,60Hz
	1280x1024,48bit,60Hz
	1366x768,24bit,60Hz
	1440x900,48bit,60Hz
	1600x1200,48bit,60Hz
	1920x1080,48bit,60Hz
	1920x1200,48bit,60Hz
Select LCD panel used.	
CH7511B Backlight Control Mode	**DC Mode**
	PWM Mode
Select CH7511B Backlight Control by DC or PWM Mode.	
Brightness Setting	**100%**
	75%
	50%
	25%
CH7511B Brightness Setting	

Memory Configuration



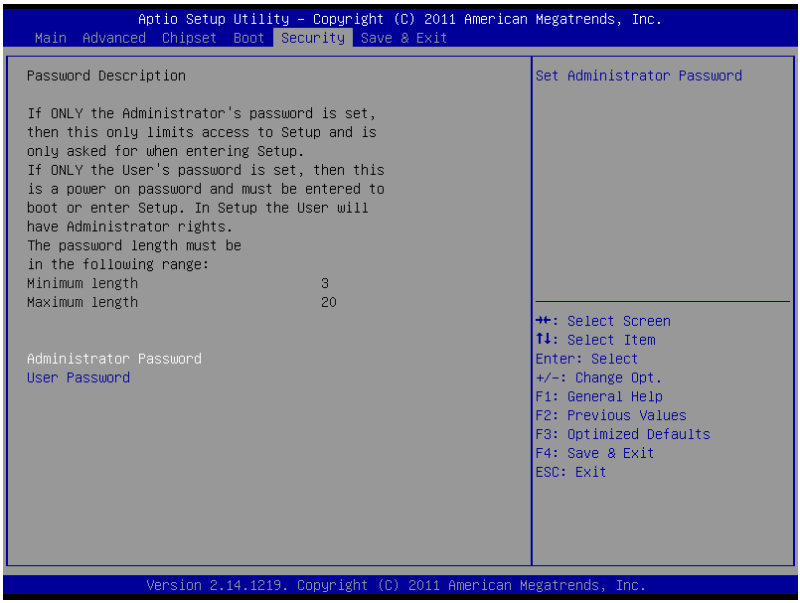
Boot



Options summary :

Quite Boot	Disabled
	Enabled
Enables or disables Quiet Boot option.	
Launch I218LM PXE OpROM	**Disabled**
	Enabled
Enabled or Disable Legacy Boot Option for I218LM.	
Launch RTL8111E PXE OpROM	**Disabled**
	Enabled
Enabled or Disable Legacy Boot Option for RTL8111E.	

Security



Change User/Supervisor Password

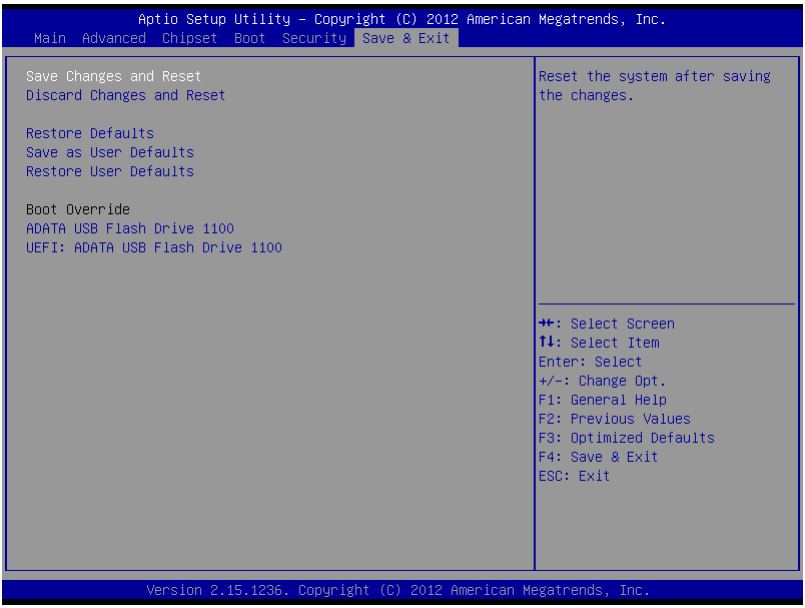
You can install a Supervisor password, and if you install a supervisor password, you can then install a user password. A user password does not provide access to many of the features in the Setup utility.

If you highlight these items and press Enter, a dialog box appears which lets you enter a password. You can enter no more than six letters or numbers. Press Enter after you have typed in the password. A second dialog box asks you to retype the password for confirmation. Press Enter after you have retyped it correctly. The password is required at boot time, or when the user enters the Setup utility.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

Setup submenu: Exit



Chapter

4

Driver Installation

.

The EMB-QM87A comes with an AutoRun DVD-ROM that contains all drivers and utilities that can help you to install the driver automatically.

Insert the driver DVD, the driver DVD-title will auto start and show the installation guide. If not, please follow the sequence below to install the drivers.

Follow the sequence below to install the drivers:

Step 1 – Install INF Driver

Step 2 – Install VGA Driver

Step 3 – Install USB3.0 Driver

Step 4 – Install Audio Driver

Step 5 – Install LAN Driver

Step 6 – Install RAID & AHCI Driver

Step 7 – Install ME Driver

Step 8 – Install TPM Driver

Step 9 – Install UART Driver (Optional)

Please read instructions below for further detailed installations.

4.1 Installation:

Insert the EMB-QM87A DVD-ROM into the DVD-ROM drive. And install the drivers from Step 1 to Step 9 in order.

Step 1 – Install Chipset Driver

1. Click on the ***Step 1-INF*** folder and double click on the ***infinst_autol.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 2 – Install VGA Driver

1. Click on the ***Step 2-VGA*** folder and select the OS folder your system is
2. Double click on the ***Setup.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 3 – Install USB3.0 Driver

1. Click on the ***Step 5-USB3.0*** folder and double click on the ***Setup.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 4 – Install Audio Driver

1. Click on the ***Step 4- Audio*** folder and select the OS folder your system is
2. Double click on the ***.exe*** located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 5 – Install LAN Driver

1. Click on the ***Step 5-LAN*** folder and select the folder of LAN chip the system adopted
2. Select the OS folder your system is and double click on the ***.exe*** file located in each OS folder
3. Follow the instructions that the window shows
4. The system will help you install the driver automatically

Step 6 – Install RAID & AHCI Driver

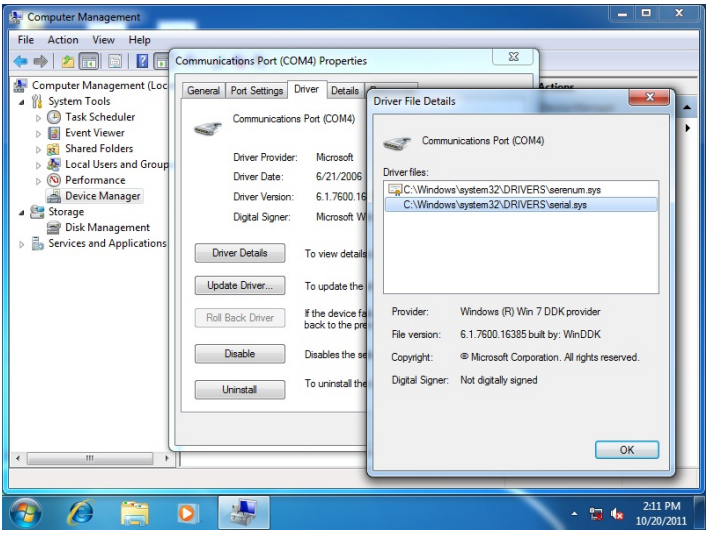
If you use AHCI or RAID mode to install your OS, you can run the ***SetupRST.exe*** located in the folder.

Step 7 – Install ME Driver

1. Click on the ***Step 7-ME*** folder and double click on the ***setup.exe*** file
2. Follow the instructions that the window shows
3. The system will help you install the driver automatically

Step 8 – Install TPM Driver

4. Click on the ***STEP8-TPM*** folder and select the OS folder your system is
5. Double click on the ***Setup.exe*** file
6. Follow the instructions that the window shows
7. The system will help you install the driver automatically



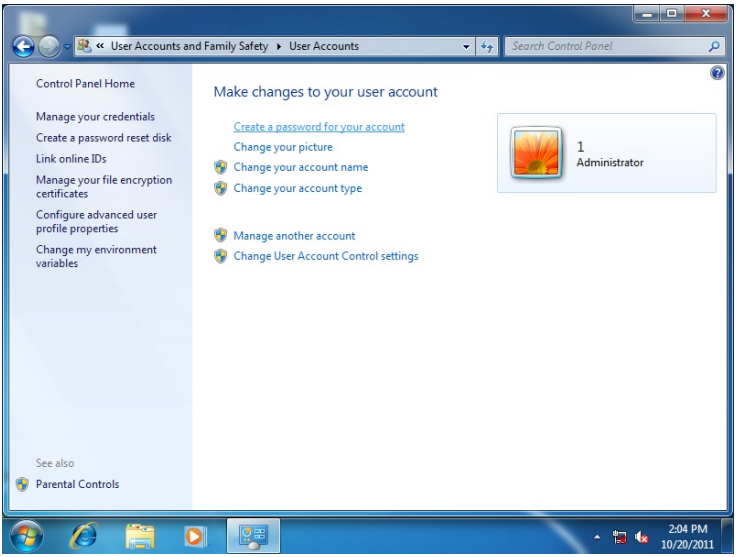
Step 9 – Install UART Driver (Optional)

For Windows® XP

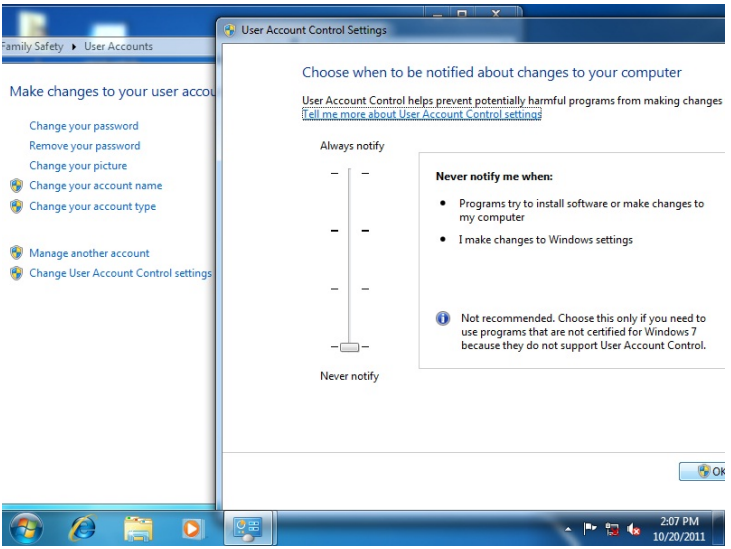
1. Click on the ***STEP9-UART*** folder and double click on ***patch.bat*** file
2. Follow the instructions that the window shows
3. The system will help you to install the driver automatically

For Windows® 7

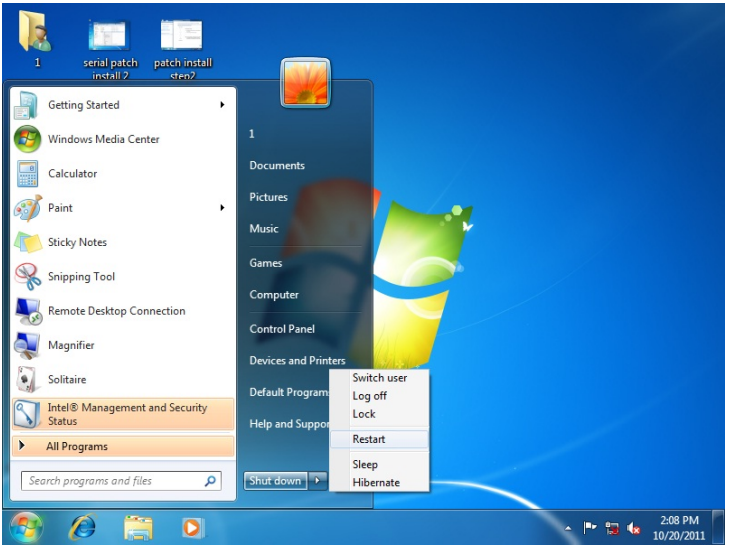
1. Create a password for Administrator account.



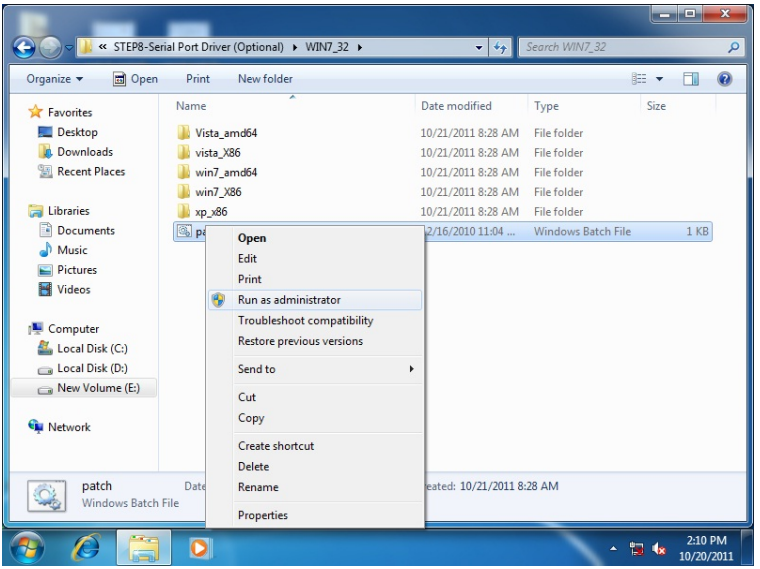
2. Change User Account Control Settings to [Never notify]

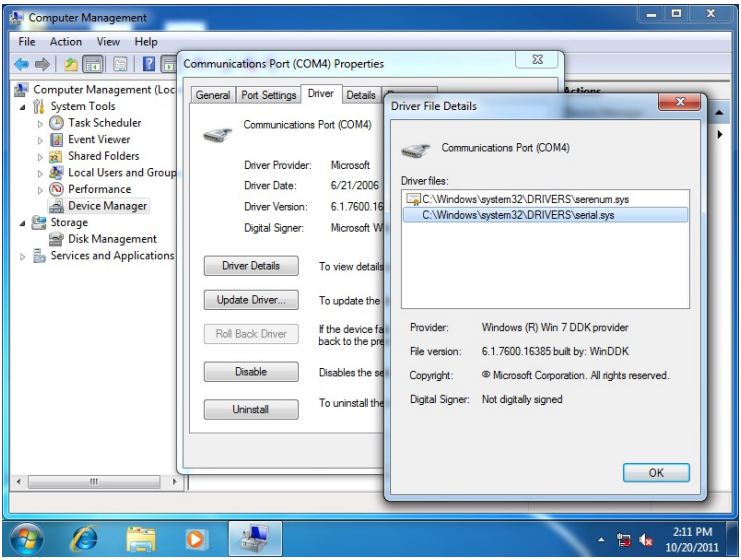


3. Reboot and Administrator login.



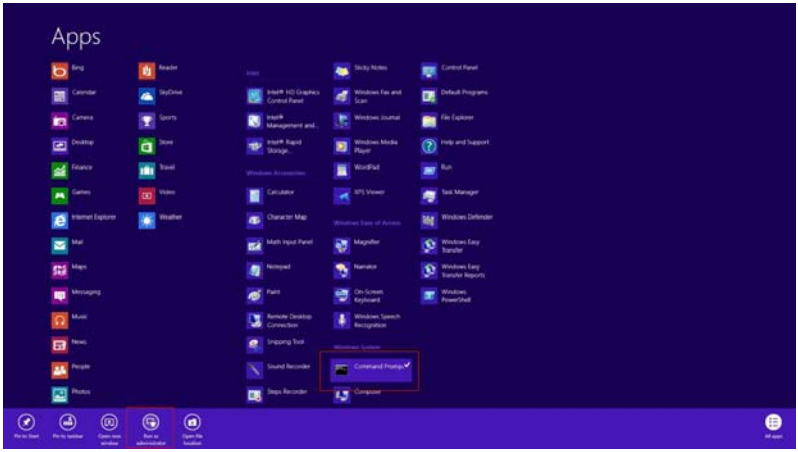
4. To run patch.bat with [Run as administrator].



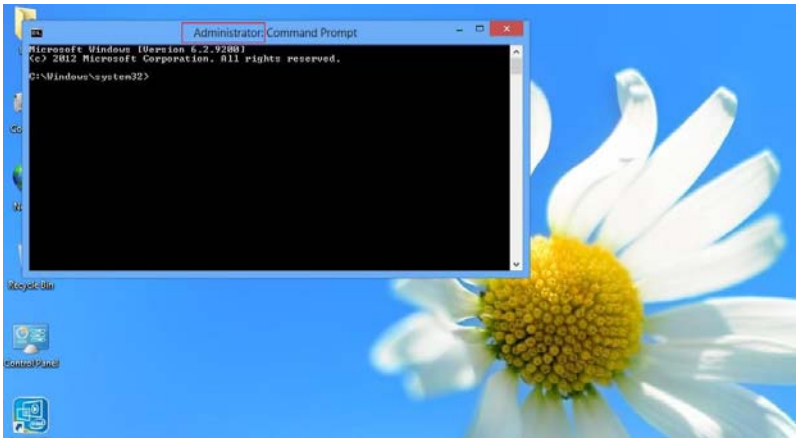


For Windows® 8

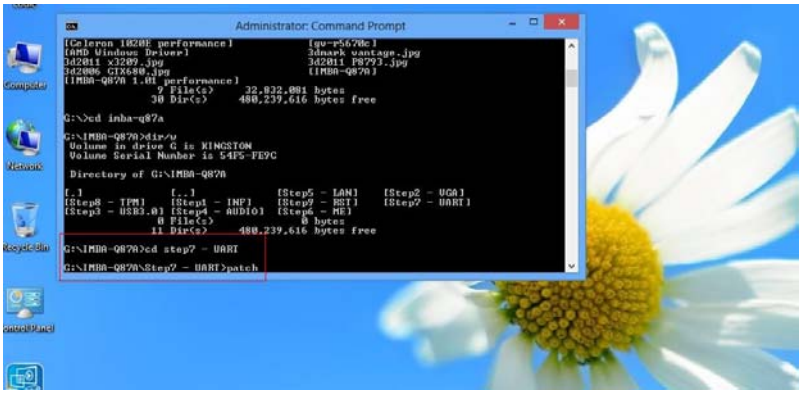
1. Right click [Command Prompt] and [run as administrator]



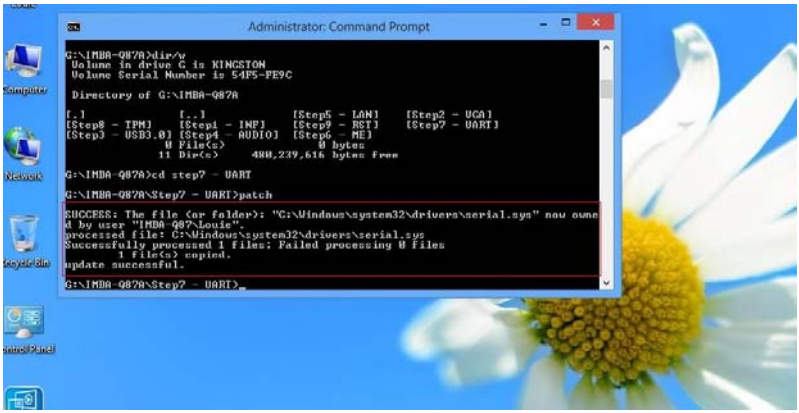
2. Run Command Prompt by administrator.



3. Run patch.bat in UART driver folder path.

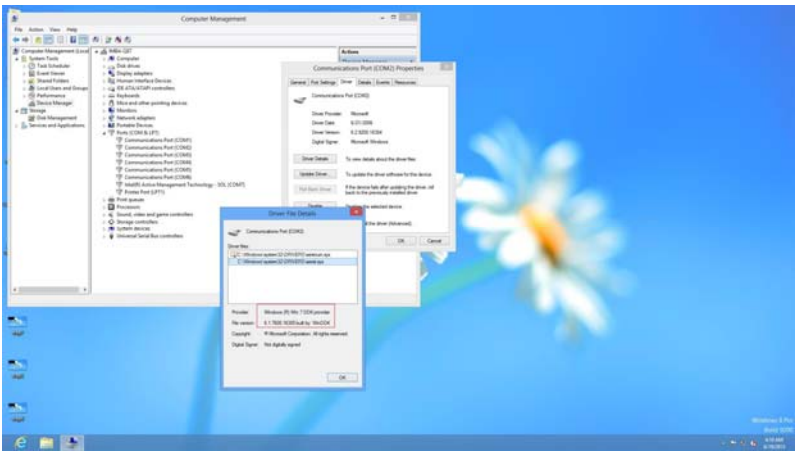


4. Update successful.



5. Restart.

6. Com port driver\serial.sys, provider will change to [Windows(R) Win7 DDK provider].



Appendix

A

Programming the Watchdog Timer

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	**Note**
Index	**0x2E**(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	**0x2F**(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	**Register**	**BitNum**	**Value**	**Note**
Timer Counter	**0x07**(Note3)	**0xF6**(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	**0x07**(Note5)	**0xF5**(Note6)	**3**(Note7)	**0**(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	**0x07**(Note9)	**0xF5**(Note10)	**5**(Note11)	**1**(Note12)	0: Disable 1: Enable
Timeout Status	**0x07**(Note13)	**0xF5**(Note14)	**6**(Note15)	**1**	1: Clear timeout status
Output Mode	**0x07**(Note16)	**0xF5**(Note17)	**4**(Note18)	**1**(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	**0x07**(Note20)	**0xFA**(Note21)	**0**(Note22)	**1**(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```
*******************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN    //This parameter is represented from Note3
#define byte   TimerReg    //This parameter is represented from Note4
#define byte   TimerVal    // This parameter is represented from Note24
#define byte   UnitLDN     //This parameter is represented from Note5
#define byte   UnitReg     //This parameter is represented from Note6
#define byte   UnitBit     //This parameter is represented from Note7
#define byte   UnitVal     //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN     // This parameter is represented from Note16
#define byte   ModeReg     // This parameter is represented from Note17
#define byte   ModeBit     // This parameter is represented from Note18
#define byte   ModeVal     // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
*******************************************************************************
```

```
**********************************************************************************
VOID   Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
        // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
**********************************************************************************
```

```
**************************************************************************************
// Procedure : AaeonWDTEnable
VOID   AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID   AaeonWDTConfig (){
        // Disable WDT counting
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
        // Clear Watchdog Timeout Status
        WDTClearTimeoutStatus();
        // WDT relative parameter setting
        WDTParameterSetting();
}

VOID   WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID   WDTParameterSetting(){
        // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
        // WDT counting unit setting
        SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
        // WDT output mode setting, level / pulse
        SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID   WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
**************************************************************************************
```

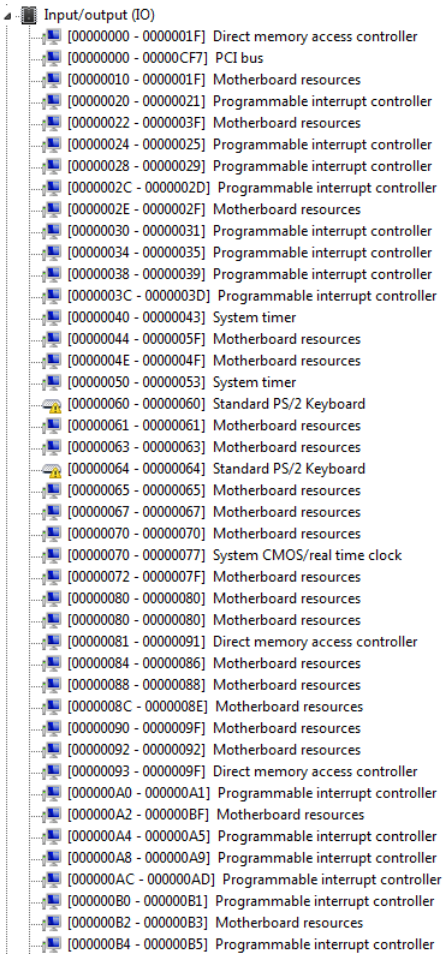
```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

Appendix

B

I/O Information

B.1 I/O Address Map

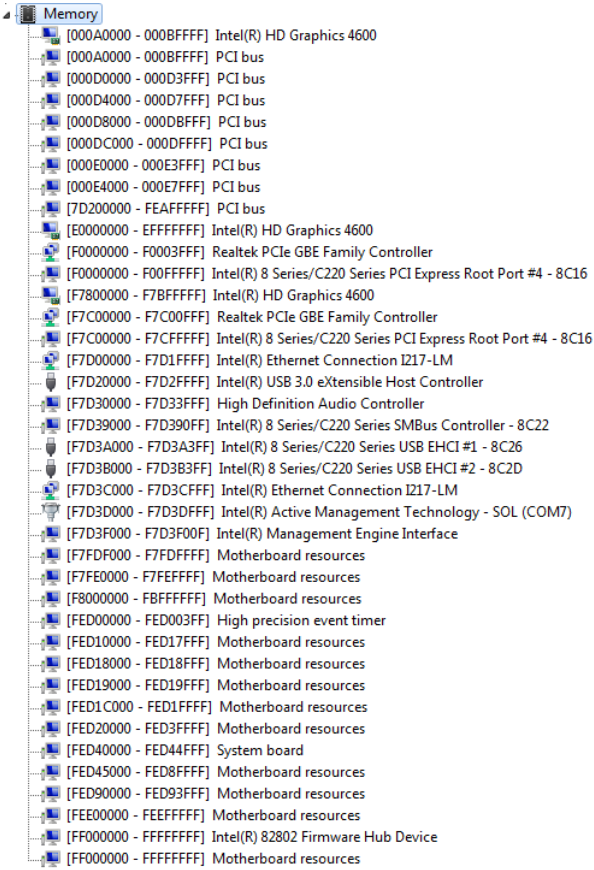


- [000000B8 - 000000B9] Programmable interrupt controller
- [000000BC - 000000BD] Programmable interrupt controller
- [000000C0 - 000000DF] Direct memory access controller
- [000000E0 - 000000EF] Motherboard resources
- [000000F0 - 000000F0] Numeric data processor
- [00000290 - 0000029F] Motherboard resources
- [000002C0 - 000002C7] Communications Port (COM6)
- [000002D0 - 000002D7] Communications Port (COM5)
- [000002E8 - 000002EF] Communications Port (COM4)
- [000002F8 - 000002FF] Communications Port (COM2)
- [000003B0 - 000003BB] Intel(R) HD Graphics 4600
- [000003C0 - 000003DF] Intel(R) HD Graphics 4600
- [000003E8 - 000003EF] Communications Port (COM3)
- [000003F8 - 000003FF] Communications Port (COM1)
- [000004D0 - 000004D1] Motherboard resources
- [000004D0 - 000004D1] Programmable interrupt controller
- [00000680 - 0000069F] Motherboard resources
- [00000A00 - 00000A0F] Motherboard resources
- [00000A10 - 00000A1F] Motherboard resources
- [00000D00 - 0000FFFF] PCI bus
- [0000164E - 0000164F] Motherboard resources
- [00001800 - 000018FE] Motherboard resources
- [00001854 - 00001857] Motherboard resources
- [00001C00 - 00001CFE] Motherboard resources
- [00001D00 - 00001DFE] Motherboard resources
- [00001E00 - 00001EFE] Motherboard resources
- [00001F00 - 00001FFE] Motherboard resources
- [0000E000 - 0000E0FF] Realtek PCIe GBE Family Controller
- [0000E000 - 0000EFFF] Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
- [0000F000 - 0000F03F] Intel(R) HD Graphics 4600
- [0000F040 - 0000F05F] Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
- [0000F080 - 0000F08F] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
- [0000F090 - 0000F09F] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
- [0000F0A0 - 0000F0A3] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
- [0000F0B0 - 0000F0B7] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
- [0000F0C0 - 0000F0C3] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
- [0000F0D0 - 0000F0D7] Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
- [0000F0E0 - 0000F0E7] Intel(R) Active Management Technology - SOL (COM7)
- [0000FFFF - 0000FFFF] Motherboard resources
- [0000FFFF - 0000FFFF] Motherboard resources
- [0000FFFF - 0000FFFF] Motherboard resources

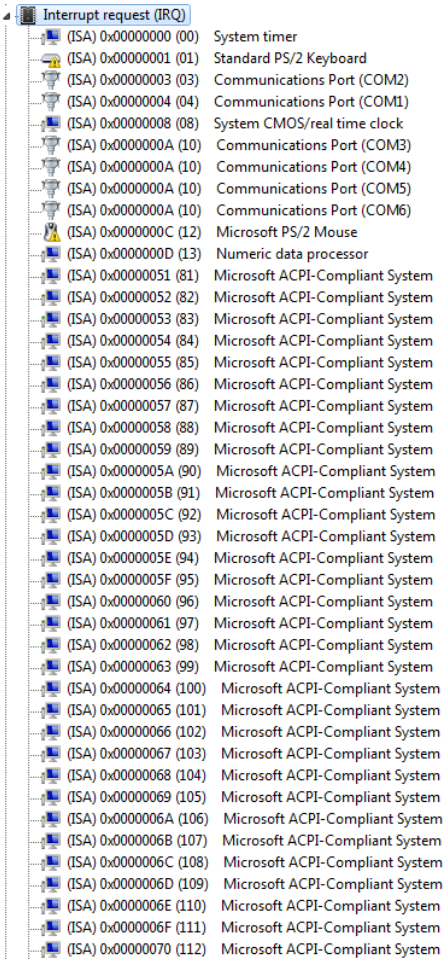
Interrupt request (IRQ)

- (ISA) 0x00000000 (00) System timer
- (ISA) 0x00000001 (01) Standard PS/2 Keyboard

B.2 Memory Address Map

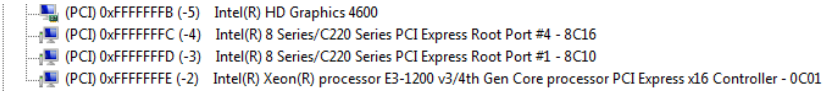


B.3 IRQ Mapping Chart

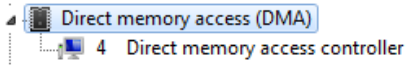


- (ISA) 0x00000071 (113) Microsoft ACPI-Compliant System
- (ISA) 0x00000072 (114) Microsoft ACPI-Compliant System
- (ISA) 0x00000073 (115) Microsoft ACPI-Compliant System
- (ISA) 0x00000074 (116) Microsoft ACPI-Compliant System
- (ISA) 0x00000075 (117) Microsoft ACPI-Compliant System
- (ISA) 0x00000076 (118) Microsoft ACPI-Compliant System
- (ISA) 0x00000077 (119) Microsoft ACPI-Compliant System
- (ISA) 0x00000078 (120) Microsoft ACPI-Compliant System
- (ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
- (ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
- (ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
- (ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
- (ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
- (ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
- (ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
- (ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
- (ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
- (ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
- (ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
- (ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
- (ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
- (ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
- (ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
- (ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
- (ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
- (ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
- (ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
- (ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
- (ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
- (ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
- (ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
- (ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
- (ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
- (ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
- (ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
- (ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
- (ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
- (ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
- (ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
- (ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
- (ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
- (ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
- (ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
- (ISA) 0x0000009C (156) Microsoft ACPI-Compliant System

- (ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
- (ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
- (ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
- (ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
- (ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
- (ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
- (ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
- (ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
- (ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
- (ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
- (ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
- (ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
- (ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
- (ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
- (ISA) 0x000000AB (171) Microsoft ACPI-Compliant System
- (ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
- (ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
- (ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
- (ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
- (ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
- (ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
- (ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
- (ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System
- (ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
- (ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
- (ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
- (ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
- (ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
- (ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
- (ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
- (ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
- (ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
- (ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
- (ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
- (PCI) 0x00000005 (05) Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
- (PCI) 0x00000010 (16) Intel(R) 8 Series/C220 Series USB EHCI #2 - 8C2D
- (PCI) 0x00000010 (16) Intel(R) Management Engine Interface
- (PCI) 0x00000013 (19) Intel(R) 8 Series 4 port Serial ATA Storage Controller - 8C01
- (PCI) 0x00000013 (19) Intel(R) Active Management Technology - SOL (COM7)
- (PCI) 0x00000016 (22) High Definition Audio Controller
- (PCI) 0x00000017 (23) Intel(R) 8 Series/C220 Series USB EHCI #1 - 8C26
- (PCI) 0xFFFFFFF8 (-8) Realtek PCIe GBE Family Controller
- (PCI) 0xFFFFFFF9 (-7) Intel(R) Ethernet Connection I217-LM
- (PCI) 0xFFFFFFFA (-6) Intel(R) USB 3.0 eXtensible Host Controller


(PCI) 0xFFFFFFFB (-5) Intel(R) HD Graphics 4600
(PCI) 0xFFFFFFFC (-4) Intel(R) 8 Series/C220 Series PCI Express Root Port #4 - 8C16
(PCI) 0xFFFFFFFD (-3) Intel(R) 8 Series/C220 Series PCI Express Root Port #1 - 8C10
(PCI) 0xFFFFFFFE (-2) Intel(R) Xeon(R) processor E3-1200 v3/4th Gen Core processor PCI Express x16 Controller - 0C01

B.4 DMA Channel Assignments



Appendix

C

Mating Connector

C.1 List of Mating Connectors and Cables

The table notes mating connectors and available cables.

Connector Label	Function	Mating Connector		Available Cable	Cable P/N
		Vendor	Model No.		
CN22	+12V AUX power connector	PINREX	740-81-08TVY8		
CN6, CN9	4 Pin FAN connector	PINREX	744-81-04TG20		
COM2 ~ COM6	COM port connector	PINREX	522-90-10GBE0		
DIO1	Digital I/O Pin Header	PINREX	222-97-05GBE1		
FP1	Front panel pin header	Astron	27-06061-205-1G-1-R		
CN21	LVDS panel power connector	PINREX	721-81-05TW00		
LVDS1	LVDS panel connector	PINREX	712-76-30GWE0		
PCIE1	PCI-E X16 slot	FOXCONN	2EG08217-D2D-DF		
CN3, CN10	Serial ATA power Connector	HO-BASE	P201-04	SATA power cable	1702151201

SATA1, SATA2, SATA5, SATA6.	SATA III Connector	PINREX	770-83-07SV29	SATA CABLE	1709070800
SATA3, SATA4.	SATA II Connector	PINREX	770-83-07SG29	SATA CABLE	1709070800
USB1, USB2	USB2.0 pin header	PINREX	222-97-05GBE1		
CN14	USB3.0 pin header	PINREX	52X-40-20GV52		

Note: The AAEON Cable P/N with " * " sign is for WiTAS series products.

Appendix

D

Electrical Specifications for I/O Ports

D.1 DIO Programming

EMB-QM87A utilizes FINTEK 81866 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.(These three steps are the same as programming WDT)

D.2 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	**Note**
Index	**0x2E**(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	**0x2F**(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	**Register**	**BitNum**	**Value**	**Note**
DIO-1 Pin Status	**0x06**(Note3)	**0x82**(Note4)	**0**(Note5)		GPIO70
DIO-2 Pin Status	**0x06**(Note6)	**0x82**(Note7)	**1**(Note8)		GPIO71
DIO-3 Pin Status	**0x06**(Note9)	**0x82**(Note10)	**2**(Note11)		GPIO72
DIO-4 Pin Status	**0x06**(Note12)	**0x82**(Note13)	**3**(Note14)		GPIO73
DIO-5 Pin Status	**0x06**(Note15)	**0x82**(Note16)	**4**(Note17)		GPIO74
DIO-6 Pin Status	**0x06**(Note18)	**0x82**(Note19)	**5**(Note20)		GPIO75
DIO-7 Pin Status	**0x06**(Note21)	**0x82**(Note22)	**6**(Note23)		GPIO76
DIO-8 Pin Status	**0x06**(Note24)	**0x82**(Note25)	**7**(Note26)		GPIO77

Table 3 : Digital Output relative register table					
	LDN	**Register**	**BitNum**	**Value**	**Note**
DIO-1 Output Data	**0x06**(Note27)	**0x88**(Note28)	**0**(Note29)	(Note30)	GPIO70
DIO-2 Output Data	**0x06**(Note31)	**0x88**(Note32)	**1**(Note33)	(Note34)	GPIO71
DIO-3 Output Data	**0x06**(Note35)	**0x88**(Note36)	**2**(Note37)	(Note38)	GPIO72
DIO-4 Output Data	**0x06**(Note39)	**0x88**(Note40)	**3**(Note41)	(Note42)	GPIO73
DIO-5 Output Data	**0x06**(Note43)	**0x88**(Note44)	**4**(Note45)	(Note46)	GPIO74
DIO-6 Output Data	**0x06**(Note47)	**0x88**(Note48)	**5**(Note49)	(Note50)	GPIO75
DIO-7 Output Data	**0x06**(Note51)	**0x88**(Note52)	**6**(Note53)	(Note54)	GPIO76
DIO-8 Output Data	**0x06**(Note55)	**0x88**(Note56)	**7**(Note57)	(Note58)	GPIO77

D.3 Digital I/O Sample Program

```
**********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte    SIOIndex    //This parameter is represented from Note1
#define byte    SIOData     //This parameter is represented from Note2
#define   void    IOWriteByte(byte IOPort, byte Value);
#define   byte    IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte    DInput1LDN    // This parameter is represented from Note3
#define byte    DInput1Reg    // This parameter is represented from Note4
#define byte    DInput1Bit    // This parameter is represented from Note5
#define byte    DInput2LDN    // This parameter is represented from Note6
#define byte    DInput2Reg    // This parameter is represented from Note7
#define byte    DInput2Bit    // This parameter is represented from Note8
#define byte    DInput3LDN    // This parameter is represented from Note9
#define byte    DInput3Reg    // This parameter is represented from Note10
#define byte    DInput3Bit    // This parameter is represented from Note11
#define byte    DInput4LDN    // This parameter is represented from Note12
#define byte    DInput4Reg    // This parameter is represented from Note13
#define byte    DInput4Bit    // This parameter is represented from Note14
#define byte    DInput5LDN    // This parameter is represented from Note15
#define byte    DInput5Reg    // This parameter is represented from Note16
#define byte    DInput5Bit    // This parameter is represented from Note17
#define byte    DInput6LDN    // This parameter is represented from Note18
#define byte    DInput6Reg    // This parameter is represented from Note19
#define byte    DInput6Bit    // This parameter is represented from Note20
#define byte    DInput7LDN    // This parameter is represented from Note21
#define byte    DInput7Reg    // This parameter is represented from Note22
#define byte    DInput7Bit    // This parameter is represented from Note23
#define byte    DInput8LDN    // This parameter is represented from Note24
#define byte    DInput8Reg    // This parameter is represented from Note25
#define byte    DInput8Bit    // This parameter is represented from Note26
**********************************************************************************
```

```
**********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
**********************************************************************************
```

```
**************************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //        Example, Read Digital I/O Pin 3 status
        // Output :
        //        InputStatus :
        //                0: Digital I/O Pin level is low
        //                1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //        Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit, DOutput6Val);
}
**************************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
        IOWriteByte(SIOIndex, 0x87);
        IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
        IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
        IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= ~(1 << BitNum);
        TmpValue |= (Value << BitNum);
        IOWriteByte(SIOData, TmpValue);
        SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

```
*****************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, Register);
        TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID    ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
        IOWriteByte(SIOIndex, OutputEnableReg);
        TmpValue = IOReadByte(SIOData);
        TmpValue |= (1 << BitNum);
        IOWriteByte(SIOData, OutputEnableReg);
        SIOExitMBPnPMode();
}
*****************************************************************************
```